**Overview**

UMC’s Design Support Solutions provide customers with a practical and cost-effective environment from RTL designs to GDSII tape-outs. The fundamental IP solutions include speed and area optimized standard cell libraries, I/O libraries with patented ESD protection, and embedded memory compilers. The platform-based IP solutions enable customers to easily develop specific products such as baseband chips, DTV controllers, audio player controllers, digital camera controllers, etc. The low power design flow provides customers with a quick start for SoC designs in advanced technologies. Cost effective DFM solutions offer customers practical DFM methodologies that are seamlessly compliant with current SoC designs flows. The foundry design kits provide customers a quick and convenient analog design environment with Optimized Capacitor Finder (OCF), Optimized Inductor Finder (OIF) and Optimized Transformer Finder (OTF).

**Fundamental IP**

**Standard Cell Libraries**
UMC’s standard cell libraries are optimized for UMC’s advanced technologies including 90nm, 65nm, 40nm and 28nm. They provide rich features including multiple threshold voltage support, over-drive capabilities, density up to 3120 K-gate/mm² at 28nm, multi-Vdd operations, and DFM compliance.

**Standard I/O Libraries**
With patented ESD protection techniques, UMC’s standard I/O libraries provide the best functionality for SoC connectivity. In addition to 16mA fan-out driving, the I/O cells have a compact cell area at advanced nodes with Bonding Over Active Circuit (BOAC) support. Analog I/O & power cells are also available.

**Embedded Memory Compilers**
Embedded memories are generally required for SoC designs. UMC offers complete embedded memory generators for designers’ convenience. These include single port SRAM, dual port SRAM, 1-port register files, 2-port register files, and ROM. The bit cells are built with HVt or Rvt MOS transistors for low power designs in advanced technologies.
**ANALOG IP**

**Platform based IP solutions**
With a complete platform based IP portfolio, customers are able to seamlessly deploy their required IP for specific SoC products, such as baseband SoCs, digital TV controllers, camera controllers and audio players.

**Embedded Memory Macros**

In the modern SoC era, memory becomes an important and essential IP requirement for SoC design. UMC offers state-of-the-art embedded memory solutions to meet a variety of applications for 4C markets.

High quality embedded non-volatile memory (eFuse, eOTP, eMTP, eEEPROM and eFlash) can be used for trimming, redundancy, data encryption, ID, coding and programming.

In addition, UMC’s proprietary URAM™ is an ideal solution for higher density memory requirements. The important features of URAM are smaller form factor, higher bandwidth/speed and lower power consumption compared to traditional embedded 6T-SRAM.

These comprehensive IP solutions have been helping UMC customers maximize the performance potential of their SoC designs.

**UMC Embedded Memory Profiles**
UMC offers a comprehensive embedded memory profile. Customers have many options to help customize their SoC designs.

Furthermore, UMC embedded memory is logic process compatible. The logic standard cell (SC) and I/O can be adopted directly into UMC embedded memory.
Low Power Design

With today’s proliferation of low power applications, lowering energy consumption without sacrificing performance has become a critical concern for chip designers. UMC is committed to providing customers with the latest low power solutions, including low power and low leakage transistor options using advanced technologies. UMC develops multi Vt reference flows for low power designs. For advanced low power solutions, UMC provides low power kits as well as UMC libraries. Related reference EDA flows are also available upon request. These resources provide customers with a streamlined path to manufacturing, allowing UMC customers designing power-efficient SoC projects to capitalize on today’s low power market opportunities.

Low Power Design Support

To reduce overall power consumption, designers have to take action during both front-end and back-end design stages. As shown in the following chart, UMC is delivering convenient design solutions to support designers at each stage.

Low Power Design Solutions

<table>
<thead>
<tr>
<th>Type</th>
<th>Support Features</th>
<th>Support</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>28nm</td>
</tr>
<tr>
<td>Dynamic Power</td>
<td>Voltage Island &amp; Scaling</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Clock Gating &amp; Frequency Scaling</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Multi-Vt</td>
<td>✓</td>
</tr>
<tr>
<td>Le漏kage Power</td>
<td>Power Gating</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Body Bias</td>
<td>✓</td>
</tr>
</tbody>
</table>

Timing and power models will be supported according to each customer’s particular requirements.
**Low Power Reference Design Flow**

Advanced leakage reduction techniques are demonstrated with low power reference design flow examples – Multi-Vdd Design with established voltage island, Multi-Vt Optimization, and advanced power gating technologies.

**Multi-Vdd Designs**

Multi-Vdd designs are common in advanced technologies. In addition to data retention circuitry and timing considerations, UMC also supports designers to optimize voltage island placement surrounded by appropriate level shifters. The left is the example of the voltage island establishment.

**Multi-Vt Optimization**

Multi-Vt optimization can be performed using a two-phase leakage reduction flow. This enables optimized results for cell swaps, where low threshold voltage standard cells are replaced with high threshold voltage standard cells. The result is an 83% leakage power reduction in 0.13um technology.

**Experimental Results**

- Clock Speed: 333Mhz
- Gate Count: About 1 million gates
- Process: UMC 0.13um 1P8M
**Power Gating Solution**

UMC’s power gating solution takes advantage of high threshold-voltage transistors or sleep transistors in circuit blocks that switch infrequently. This results in zero standby currents during the inactive state. The goal of power gating is to minimize leakage current by temporarily switching off power to blocks that are not required in the current operating mode. In our low power kits, we also designed isolation cells to prevent crowbar current. For the advanced purpose of retaining the internal state of the block during power down and restoring the state during power up, we also implemented retention registers in place of ordinary flip-flops. The result is a 70x leakage power reduction for 65nm technology through a proper design implementation strategy.

**Foundry Design Kit (FDK)**

The Foundry Design Kit provides IC designers with an automatic design environment that eliminates unnecessary manual tasks and ensures successful mixed signal and RF IC tape-outs. The FDK includes parameterized cells (P Cell), which have a schematic layout to provide an automatic and complete design flow. Callback functions are also provided in the design flow to minimize data entry.

In addition, UMC has worked with industry leading EDA tool partners to deliver fast and accurate 3D electromagnetic simulation tools for RF chip designs, including Virtual Capacitor Library (VCL), Virtual Inductor Library (VIL), and Virtual Transformer Library (VTL). UMC has also implemented Optimized Capacitor Finder (OCF), Optimized Inductor Finder (OIF), and Optimized Transformer Finder (OTF) tools deployed inside UMC’s Foundry Design Kit (FDK). These tools allow customers to make tradeoff decision between impedance and area, Q and area, or request a specified “flatness” of inductance within a given frequency range for ultra-wideband (UWB), WiMAX, and mobile TV design.

**Using OIF for Optimum Inductor**
**Broad EDA Tool Support**

UMC works closely with leading EDA tool vendors to provide a convenient, productive and up-to-date work environment for designers. Tools are well supported by UMC and its EDA partners throughout the entire design process, from RTL design to tapeout.

### Logic Simulation
- **Cadence**: NC-Sim
- **Mentor**: ModelSim
- **Synopsys**: VCS, MVRC

### Place & Route
- **Cadence**: ETS, EPS, CELTIC
- **Mentor**: Calibre, XRC
- **Synopsys**: Hercule, StarRC-XT
- **Magma**: Calibre, XRC
- **Synopsys**: Hercule, StarRC-XT

### Logic Synthesis
- **Cadence**: RTL Compiler
- **Magma**: Talus Design, Talus Power
- **Synopsys**: Design Compiler
- **Magma**: IC Compiler, PrimeTime, PrimeRail
- **Synopsys**: Design Compiler, PrimeTime, PrimeRail

### Physical Design
- **Talus Vortex**, **Talus Power**, **Talus Design**, **Quartz Rail**

### Physical Verification
- **Cadence**: Assura, QRC
- **Mentor**: Calibre, XRC
- **Synopsys**: Hercule, StarRC-XT
- **Magma**: Quartz, QuickCap

### Customer Support

**Partnership with ARM, Faraday & Virage**
- Enables prompt response from IP vendors
- Feasibility assessment for customer’s requirements

**Free Libraries for cost-sensitive products**
- Foundry library programs

**UMC Online support environment**
- IP Master sourcing
- IP Help Desk
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