

## Notice in Usage of This Reference Flow

Dear Valued Customer,

Due to tool revision, UMC will no longer maintain this flow.

Customer may still download the datasheet and workbook from UMC website for references, but UMC will not provide the databases or scripts mentioned in above documents.

For tool usage issues in the flow, customers may contact local application engineers of related EDA vendors. Cadence customers may visit the following website for more information <http://sourcelink.cadence.com/en/help/Contacts1.jhtml>

Thanks for your kind understanding.

UMC Reference Flow Development Team

## DATASHEET

# UMC Digital Reference Flow

The UMC digital reference flow provides a top-down solution from RTL to GDSII using tools from Cadence and Mentor Graphics. Furnished with a comprehensive arsenal of EDA tool scripts and flow steps, this hierarchical flow not only resolves phenomenon encountered with UMC's 0.13um process, but also prepares designers for potential issues that might arise from deep sub-micron process technology. As such, this digital flow is intended to adapt to any customer design environment by using the highly flexible and configurable LEON-2 processor as its core to exercise its flow steps. It also offers a robust means to help increase our customers' SoC design competitiveness by accelerating their time-to-silicon and avoiding pricey re-spins. This design flow is segmented into four comprehensible phases: Design Acceptance, Design Planning, Design Implementation, and Chip Finishing.

### **Phase 1: Design Acceptance**

Prior to venturing into the design flow, rigorous checks are meticulously performed on the design & library data, timing constraints, and the intended RTL functions.

### **Phase 2: Design Planning**

In this stage, the reference design is synthesized from the RTL code to gate-level netlist. Scan chains are inserted to provide easy access to internal nodes. Silicon virtual prototyping is then performed to determine the feasibility of the netlist, floorplan, and timing constraints. Lastly, floorplanning is performed to implement a realistic chip level planning while taking into account its timing budget.

### **Phase 3: Design Implementation**

In this stage, physical implementation of blocks is performed with timing closure achieved. A sequence of actions is then conducted to complete the top and block level implementation: scan chain reordering, time-driven routing, RC extraction, clock tree synthesis, in-place optimization, filler cell insertion, SI prevention, and cross-talk analysis are some of the steps.

### **Phase 4: Chip Finishing**

The final stage refines the full chip implementation to achieve final timing closure. Full-chip extraction, final timing analysis, and physical verification are performed to ensure a clean, tapeout-ready GDSII file.

# UMC Digital Reference Flow

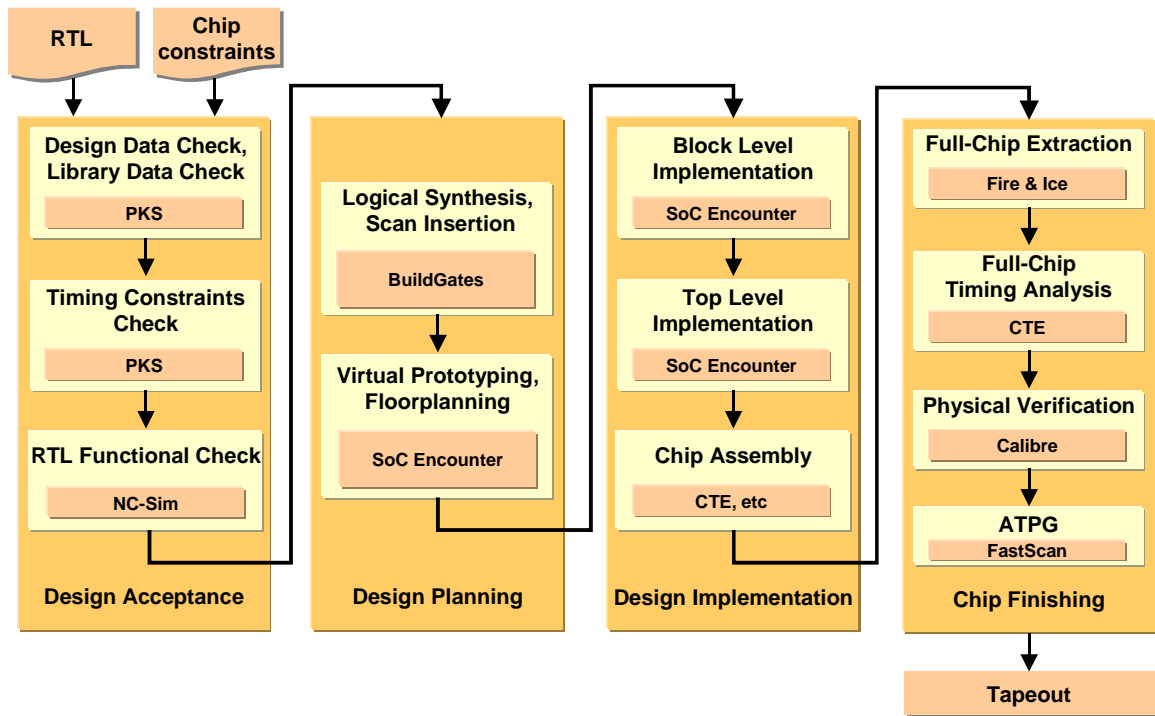


Figure 1. Overview of UMC Digital Reference Flow