

Notice in Usage of This Reference Flow

Dear Valued Customer,

Due to tool revision, UMC will no longer maintain this flow.

Customer may still download the datasheet and workbook from UMC website for references, but UMC will not maintain the databases or scripts mentioned in above documents.

For tool usage issues in the flow, customers may contact local application engineers of related EDA vendors. Cadence customers may visit the following website for more information <http://sourcelink.cadence.com/en/help/Contacts1.jhtml>

Thanks for your kind understanding.

UMC Reference Flow Development Team

UMC Multi-Vt and DFT Reference Flow

This Multi-Vt and DFT Reference Flow is the second generation of the previous LEON2 L130 reference flow. In this RTL-to-GDSII flow, new DFT features and low-power – technologies were implemented on LEON2. The front-end flow adopts latest Mentor DFT flow, which integrates MBISTArchitect, DFTAdvisor and TestKompress. The back-end implementation flow adopts the latest Cadence SoC Encounter (SoC-E) platform, which integrates First Encounter (FE), Global Physical Synthesis (GPS), and other sign-off tools into one real-time Synthesis Place and Route (SP&R) tool suite. The main purpose is to provide the user with an understanding of the in-depth DFT and low-power design flow using this SoC as a reference design. This design is segmented into four comprehensible phases : Frond-end Acceptance, Design Planning, Design Implementation, and Chip Finishing.

Phase 1: Frond-end Acceptance

To ensure a smooth design implementation, the first step is to verify the correctness of the data, which includes library data, technology data, and design data. The front-end acceptance procedures were performed for this purpose.

Phase 2: Design Planning

The major design change occurs after synthesizing design, which involves inserting memory BIST, EDT, and scans chains using Cadence RTL Compiler, Mentor MBISTArchitect, Mentor DFTAdvisor and Mentor TestKompress. Silicon Virtual Prototyping determines the feasibility of the netlist, floorplan, and constraints. More specifically, it allows you to floorplan, place and route your design in flat style, analyze timing and congestion, and refine the design to meet requirements.

Phase 3: Design Implementation

Creates physical implementations for multi-vt flow. The low-power technology will be implemented with SoC Encounter. A sequence of actions is then conducted to complete the top level implementation : scan chain recordering, time-driven placement, RC extraction, leakage power optimization, clock tree synthesis, filler cell insertion, double-cut vias, viafram, SI prevention, and crosstalk analysis are some of the steps.

Phase 4: Chip Finishing

The Chip Sign-Off process consists of bringing the detailed information for full chip extraction, power, and timing. Integrate all created physical layouts, perform final verification, and prepare the design for tape-out.

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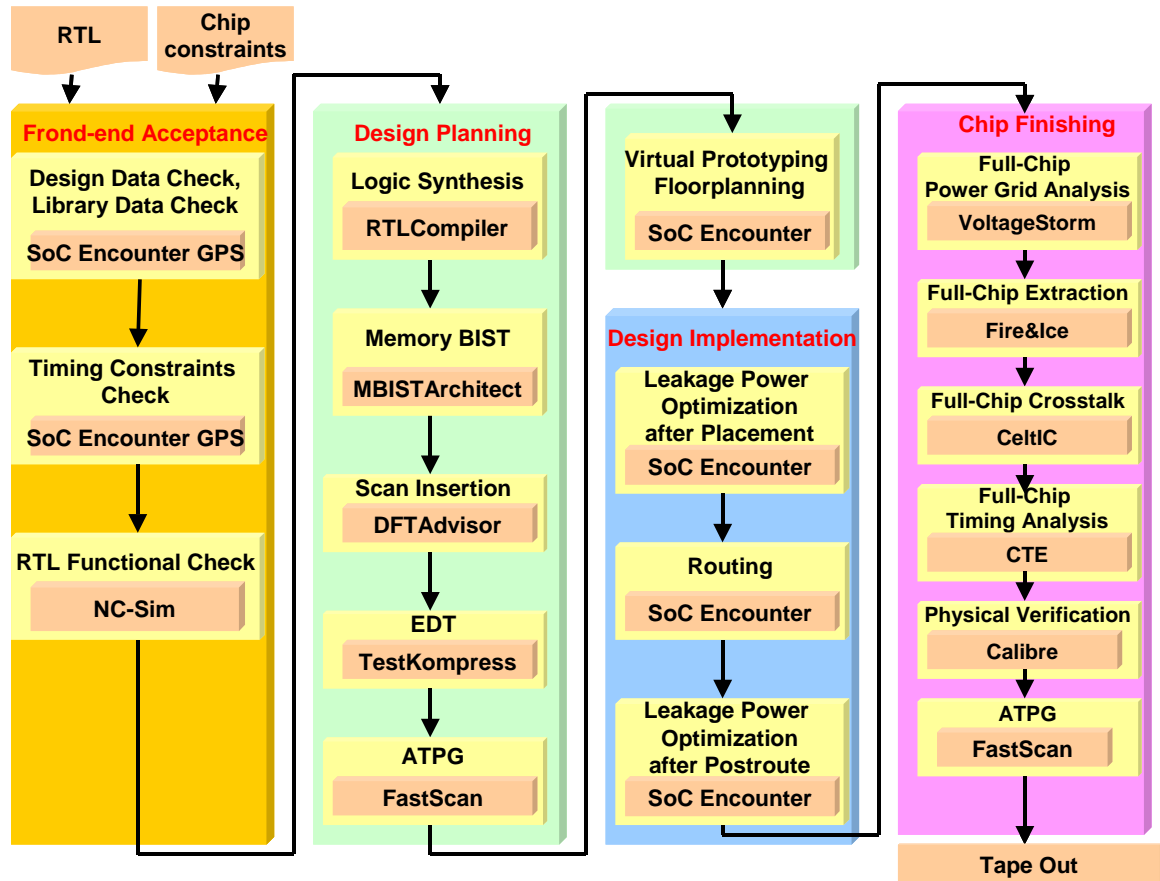


Figure 1. Overview of UMC Multi-Vt and DFT Reference Flow