FOUNDRY LEADERSHIP FOR THE SoC GENERATION

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0.13 Micron

UMC

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Key Features

- Integrated flows for Logic, Mixed-Mode/RF
- 2.28um² SRAM bit cell
- e-Fuse option
- Shallow trench isolation
- Retrograde twin well (Triple well option)
- Dual gate oxides
- $CoSi_2$ process
- Up to 1P8M Cu with FSG dielectric
- BOAC (Bonding Over Active Circuit)
- Wire Bond / Flip Chip option

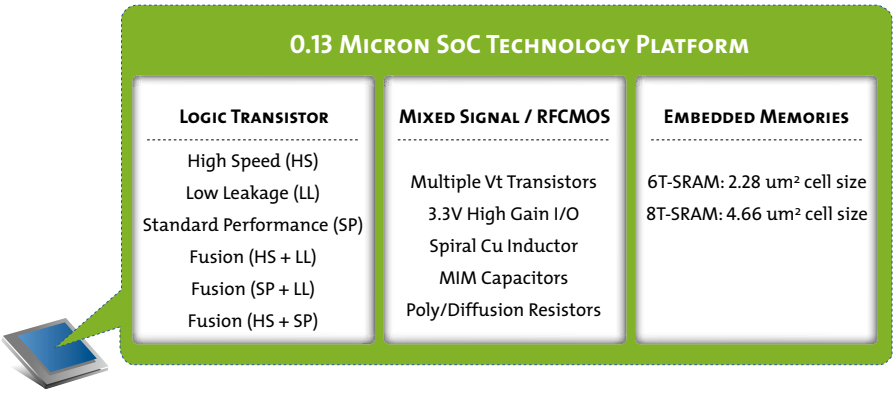
UMC's mainstream 0.13um technology is in volume production for a wide range of customer products in the computer, consumer, and communications sectors. This technology is supported by a complete SoC solution package that includes IP, library, EDA tool and other resources to help you achieve volume production of your SoC product in the shortest time possible.

Customers can also take advantage of UMC's world leading manufacturing capabilities to realize maximum competitive advantages. 300mm production and industry leading yields and cycle times ensure that you can maximize your productivity for better cost efficiencies for volume production of your design.

Furthermore, with UMC's 0.11um process, customers can enjoy lower production cost while keeping the same performance. This production proven half node technology increases gross die per wafer.

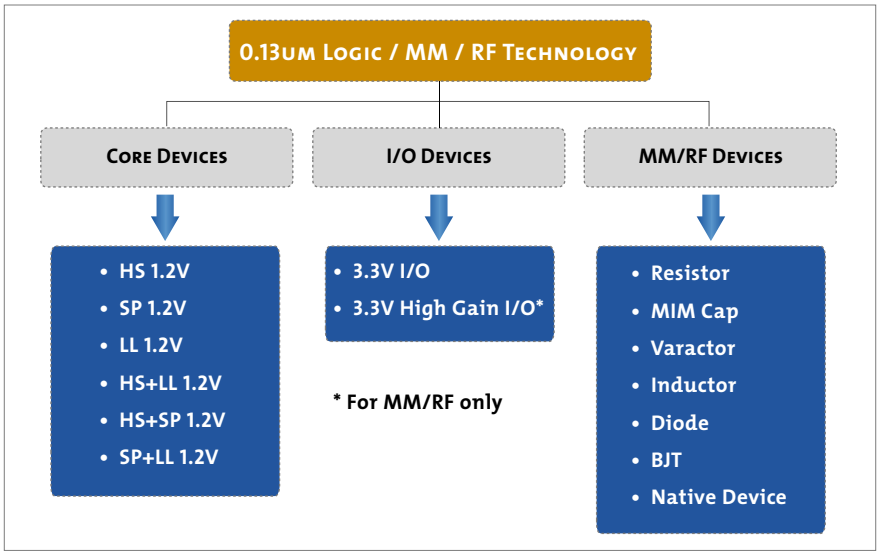
0.13um SoC Process Platform

UMC's 0.13-micron SoC solution begins with a flexible technology design platform. Customers are able to choose from a variety of process device options optimized for their specific application, such as High Speed (HS), Standard Performance (SP), Low Leakage (LL), or the unique Fusion process. Other technology options can then be implemented including mixed signal/ RFCMOS and embedded memories to further customize the process.



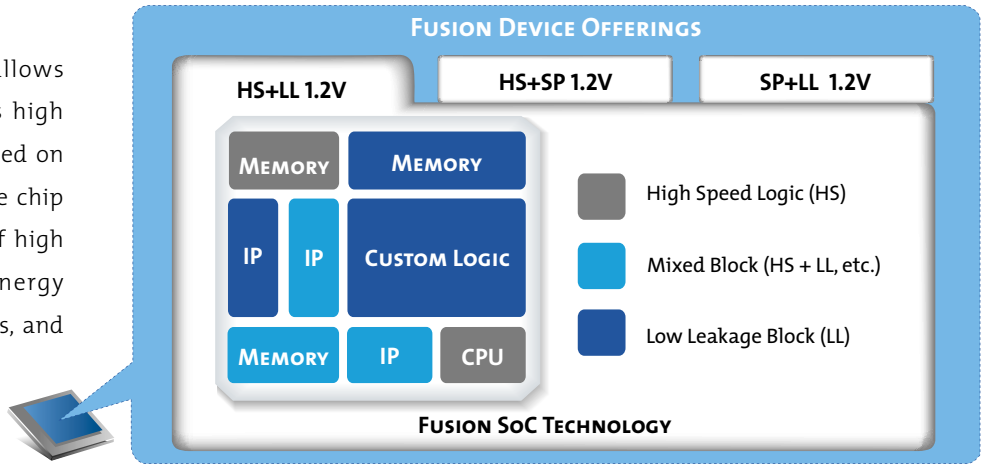
0.13um Device Offerings

UMC's 0.13um technology features a wide range of device offerings, each optimized for different product applications, from high speed to low leakage. In addition to these core offerings, RFCMOS/Mixed mode technologies are available along with Fusion, a design option that allows both high speed and low leakage transistors to be combined on a single chip.



Fusion

UMC's innovative Fusion process allows different transistor devices, such as high speed and low leakage, to be combined on the same design. This creates a single chip solution that offers the advantage of high performance without sacrificing energy efficiency, ideal for today's 3G, wireless, and portable communication products.



Silicon Verified IP Solutions

UMC offers comprehensive design resources that enable our customers to fully realize the advantages of UMC's advanced technologies. UMC's silicon verified fundamental IPs (standard cells, I/Os, and memory compilers) help customers easily migrate their designs to the next process generation to realize significant performance advantages while also reducing die size.

Customers can also leverage application specific IPs that are specialized for all types of mainstream applications such as digital TVs, cellular baseband controllers, digital cameras, and audio players to overcome time-to-market challenges.

Fundamental IP Support for SoC Designs

UMC offers comprehensive design resources that support our 0.13um process technology. Silicon verified fundamental IPs (standard cells, I/Os, and memory compilers) optimized to UMC technologies are available free-of-charge from several leading vendors.

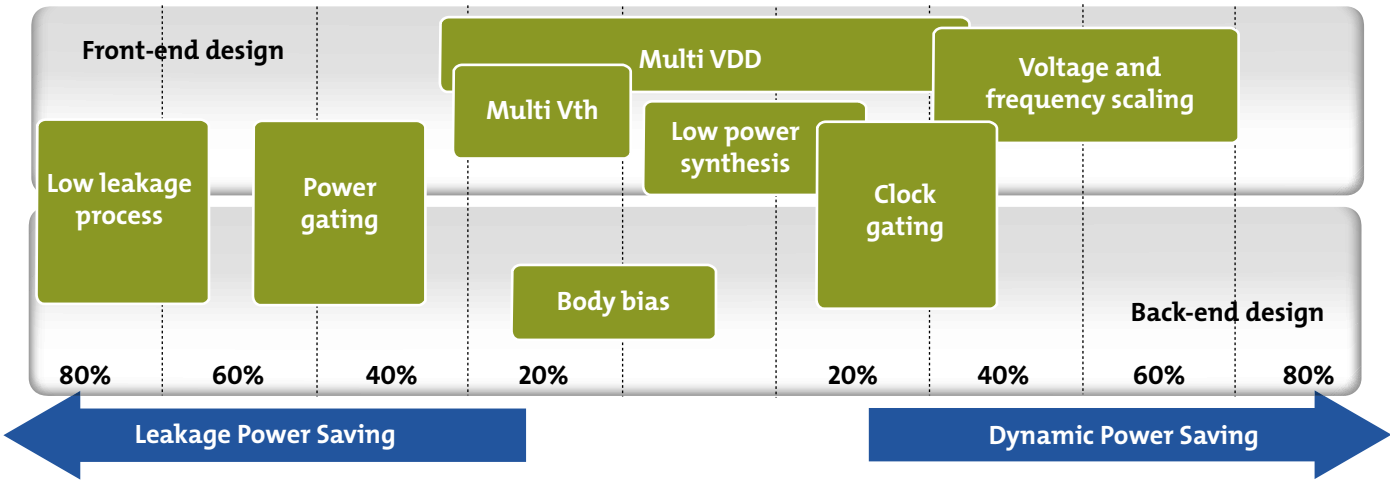
Library Provider	0.13um									
	FARADAY				VIRAGE			ARM		
Library	HS	SP	LL	Fusion	HS	SP	LL	HS	SP	LL
Standard Cells	√	√	√					√	√	√
I/O	√	√	√							
Single Port SRAM Compiler	√	√	√	√	√	√	√			
Dual Port SRAM Compiler	√	√	√	√	√	√	√			
Single Port Register File	√	√	√	√	√	√				
Dual Port Register File	√	√	√	√	√	√	√			
ROM Compiler	√	√	√	√	√	√				

Low Power Features of Standard Cell Library

With today's proliferation of low power applications, lowering energy consumption without sacrificing performance has become a critical concern for designers of power management chips for portable electronics. UMC supports its standard cell library with low power design features, including multiple Vt, clock-gating, level shifter and other features to complement the complete low power SOC solution.

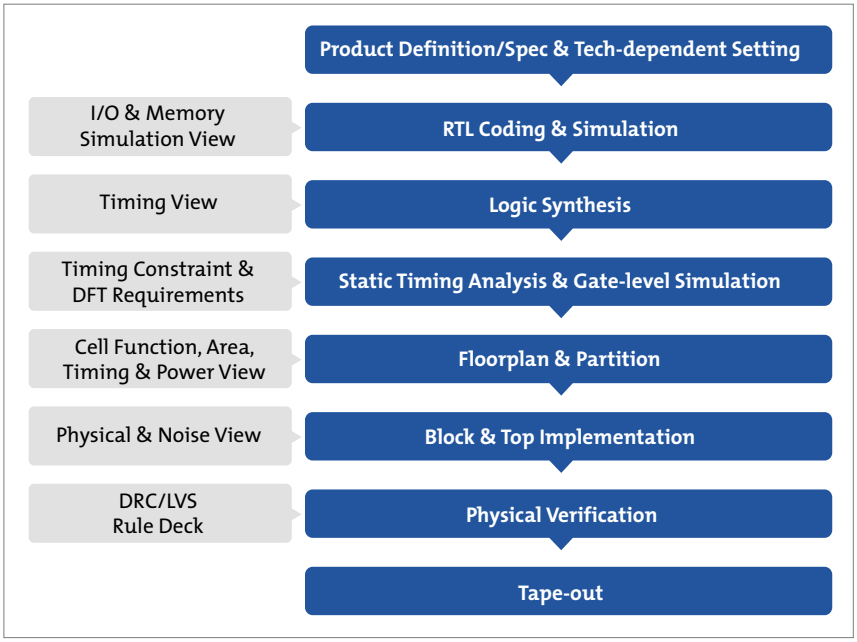
Type		Support Features		Support		
				65nm	90nm	0.13um
Operating Power	Voltage Island & Scaling	Level Shifters w / Insulator	Power & Timing Model @ 80% of Vdd	√	√	√
	Clock Gating & Frequency Scaling	Clock Gated F/F		√	√	√
Leakage Power	Multi-Vt	Multi-Vt cells		√	√	√
	Power Gating	Isolation cells, Retention F/F Headers / Footers, etc.		√	√	√
	Body Bias	Tapless cells	Timing / Power Model	√	√	√

Low Power Design Support



UMC Reference Design Flow

UMC Reference Design Flow provides a design methodology and flow validated with a "Leon2" system demonstration board. The flow incorporates 3rd-party EDA vendors' baseline design flows to address issues such as timing closure, signal integrity, leakage power and design for manufacturability and adopts a hierarchical design approach built upon silicon validated process libraries. UMC Reference Design Flow covers from schematic/RTL coding all the way to GDS-II generation and supports Cadence, Magma, Mentor and Synopsys EDA tools. All of these tools have been correlated to UMC silicon and can be interchanged for added flexibility.



Reference Design Flow and Vendor Support

UMC works with leading EDA tool companies to provide a verified Reference Design Flow program to ensure the accuracy of customer designs in a proven environment. UMC Reference Design Flow program integrates solutions for digital and analog designs and low power solutions that incorporate the latest DFM resources available from leading third-party providers. Tools can be interchanged for added flexibility.

Features of Design Flow	Cadence	Synopsys	Magma	Mentor	Ansoft	Springsoft
Functional Logic Simulation	▲	▲	-	▲	-	-
Schematic Entry	▲	-	-	-	-	-
Logic Synthesis	▲	▲	▲	-	-	-
Static Timing Analysis	▲	▲	▲	-	-	-
Timing Closure	▲	▲	▲	-	-	-
Signal Integrity	▲	▲	▲	-	-	-
Floor Planning	▲	▲	▲	-	-	-
Physical Synthesis	▲	▲	▲	-	-	-
Multi-Vt Low Power	▲	▲	▲	-	-	-
Multi-Vdd Low Power	-	▲	-	-	-	-
Design For Test	▲	▲	-	▲	-	-
Design For Diagnosis	▲	▲	-	▲	-	-
DFM - double via insertion	▲	▲	▲	-	-	-
DFM - dummy metal filling	▲	▲	▲	-	-	-
Circuits Simulation	▲	▲	-	▲	▲	-
Power Analysis	▲	▲	▲	-	-	-
Layout Editor	▲	-	-	▲	-	▲
Place & Route	▲	▲	▲	-	-	-
Physical Verification	▲	▲	-	▲	-	-
Formal Verification	▲	▲	-	-	-	-
Parasitic Extraction	▲	▲	-	▲	-	-
Noise Analysis	▲	▲	▲	-	-	-
RFCMOS/EMDM	▲	-	-	-	▲	-
Analog/Mixed Signal	▲	-	-	▲	▲	-

Note: ▲ Available

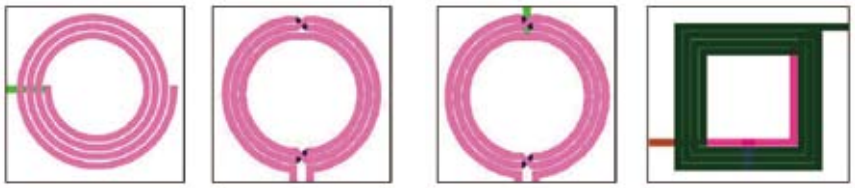
UMC e-Fuse Features

UMC has developed its own internal e-fuse solution that offers the benefits of reduced chip area, better reliability performance, and shortened repair time compared to using Al fuses. UMC not only delivers the fuse array, but also the complete functional macro for easy integration by customers. Customers may also use e-fuse for the OTP (one time programming) function to save costs.

Logic Compatible	• No extra masks necessary • Only one extra pad required
Complete Functional IP Macros	• Fuse array, programming circuit, sensing amplifier • Serial and parallel architecture
Design-Friendly Features	• Allows metal routing over fuses (M6 and above) • Programmable at package level
Flexibility	• Wafer level fuse options • Package level fuse options

Virtual Inductor Library

UMC has worked with its EDA tool partners to deliver the industry's first parameterized inductor design kit based on full-wave simulation: the Virtual Inductor Library (VIL). The VIL enables RFCMOS designers to create and simulate custom inductor geometries that are compatible with UMC's processes. It is built upon UMC's Electromagnetic Design Methodology (EMDM), which allows engineers to easily and accurately create any RF structure. EMDM gives designers the flexibility to innovate new geometries simply by editing parameters such as diameter, number of turns or width.

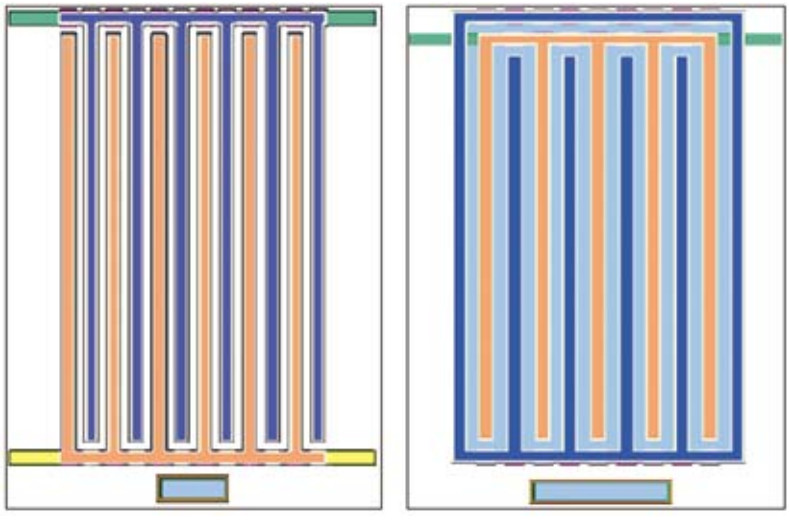


Spiral | Differential w/o center tap | Differential with center tap | Stack

The GUI based VIL can be used to simulate all types of RF inductors.

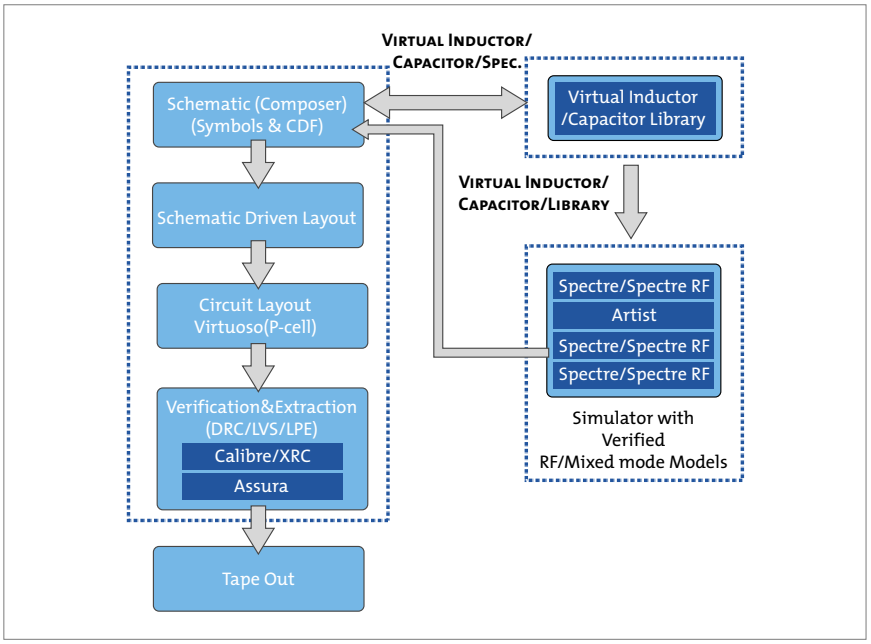
Virtual Capacitor Library

UMC has worked with its EDA tool partners to deliver the industry's first parameterized MOM capacitor design kit based on fullwave simulation: the Virtual Capacitor Library (VCL). The VCL enables RFCMOS designers to create and simulate custom capacitor geometries that are compatible with UMC's processes. It is built upon UMC's Electromagnetic Design Methodology (EMDM), which allows engineers to easily and accurately create any RF structure. EMDM gives designers the flexibility to innovate new geometries simply by editing parameters such as number of metal and fingers, arrays, and length of fingers for capacitor.



MM/RF Design Flow and FDK

The FDK (Foundry Design Kit) provides IC designers with an automatic design environment. The methodology provides access to circuit-level design and simulation, circuit layout, and layout verification with accurate RF device models. In the front-end, fundamental components of UMC's MM/RF process are implemented in common design environments and simulation tools. The back-end includes parameterized cells (P Cell), which include a schematic driven layout to provide an automatic and complete design flow. Callback functions are also provided in the design flow to minimize data entry. EDA tools for MM/RF designs are also supported.



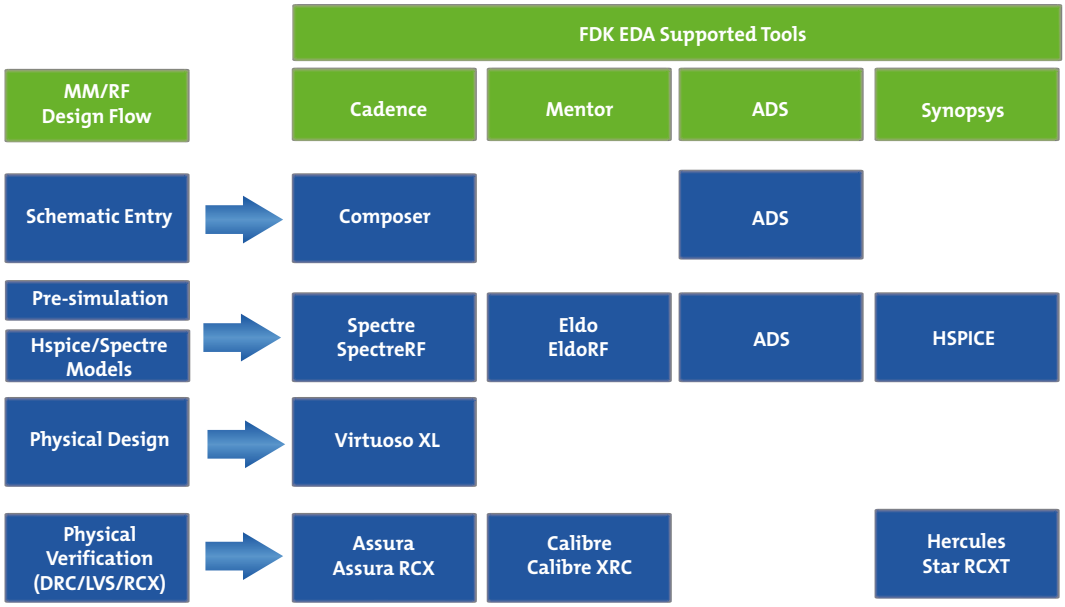
Optimum Inductor Finder (OIF)

UMC offers the Optimum Inductor Finder (OIF) in the FDK package. The OIF gives designers the ability to quickly access a large library of inductors calibrated to UMC's silicon. It also allows users to perform inductor optimization through just a few simple steps with the user-friendly interface. For instance, customers can define a desired inductance and make trade-offs between Q-factor and area. The OIF will select from its inductor library a design that best fits the specifications in a matter of seconds.

Optimum Capacitor Finder (OCF)

UMC offers the Optimum Capacitor Finder (OCF) in the FDK package. The OCF gives designers the ability to quickly access a large library of capacitors calibrated to UMC's silicon. It also allows users to perform capacitor optimization through just a few simple steps with the user-friendly interface. For instance, customers can define a desired capacitor and make trade-offs between Q-factor and area. The OCF will select from its capacitor library a design that best fits the specifications in a matter of seconds.

Analog Design Methodology



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