

Notice in Usage of This Reference Flow

Dear Valued Customer,

Due to tool revision, UMC will no longer maintain this flow.

Customer may still download the datasheet and workbook from UMC website for references, but UMC will not maintain the databases or scripts mentioned in above documents.

For tool usage issues in the flow, customers may contact local application engineers of related EDA vendors. Cadence customers may visit the following website for more information <http://sourcelink.cadence.com/en/help/Contacts1.jhtml>

Thanks for your kind understanding.

UMC Reference Flow Development Team

UMC 90 Nanometer Reference Design Flow

The UMC 90 Nanometer Reference Design Flow utilized LEON2 CPU as reference design to implement a top-down solution for an RTL-to-GDSII design flow for 90 nanometer designs targeted to address signal integrity, power integrity, and design for manufacturability (DFM) issues. The libraries play important roles in the design flow. DFM rules and technology data are incorporated into libraries in both front-end and back-end views. Thus, the entire design flow has taken DFM into consideration.

This design flow focuses on improving DFM issues by applying DFM-aware technology files. It provides an optimized approach to meet time-to-market constraints at a reduced cost. The whole flow adopts the latest Cadence SoC Encounter (SoCE) flow, which includes RTL Compiler, NC-Sim, and SoC Encounter, SignalStorm and other sign-off tools are integrated within SoC Encounter design platform tool suite. The design flow also incorporates Mentor Graphics FastScan to generate ATPG patterns and Calibre to perform physical verification.

Phase 1: Front-end Acceptance

To make sure there are no surprises during design implementation. The very first step is verifying the correctness of the data, which includes library data, technology data, and design data. The timing constraints are also checked for completeness and correctness. The design RTL code is verified to sure that the RTL function is in keeping with the initial design specification as well.

Phase 2: Design Planning

During the design-planning phase, the major steps taken involve synthesis, scan-insertion and silicon virtual prototyping. The synthesis and scan-insertion are performed with Cadence RTL Compiler. Silicon Virtual Prototyping determines the feasibility of the netlist, floorplan, and constraints. The DFM-aware libraries are used throughout these steps.

Phase 3: Design Implementation

Creates physical implementations for with SoC Encounter, which includes scan chain reordering, time-driven placement, RC extraction, leakage power optimization, clock tree synthesis, filler cell insertion, double-cut vias, viafram, SI prevention, crosstalk analysis and etc. These steps are taken with DFM recommended rules in consideration

Phase 4: Chip Finishing

The Chip Sign-Off phase involves full-chip parasitic extraction, power and timing analysis and physical verification. DFM-aware DRC and physical information are applied to ensure physical data precisely matches with actual silicon.

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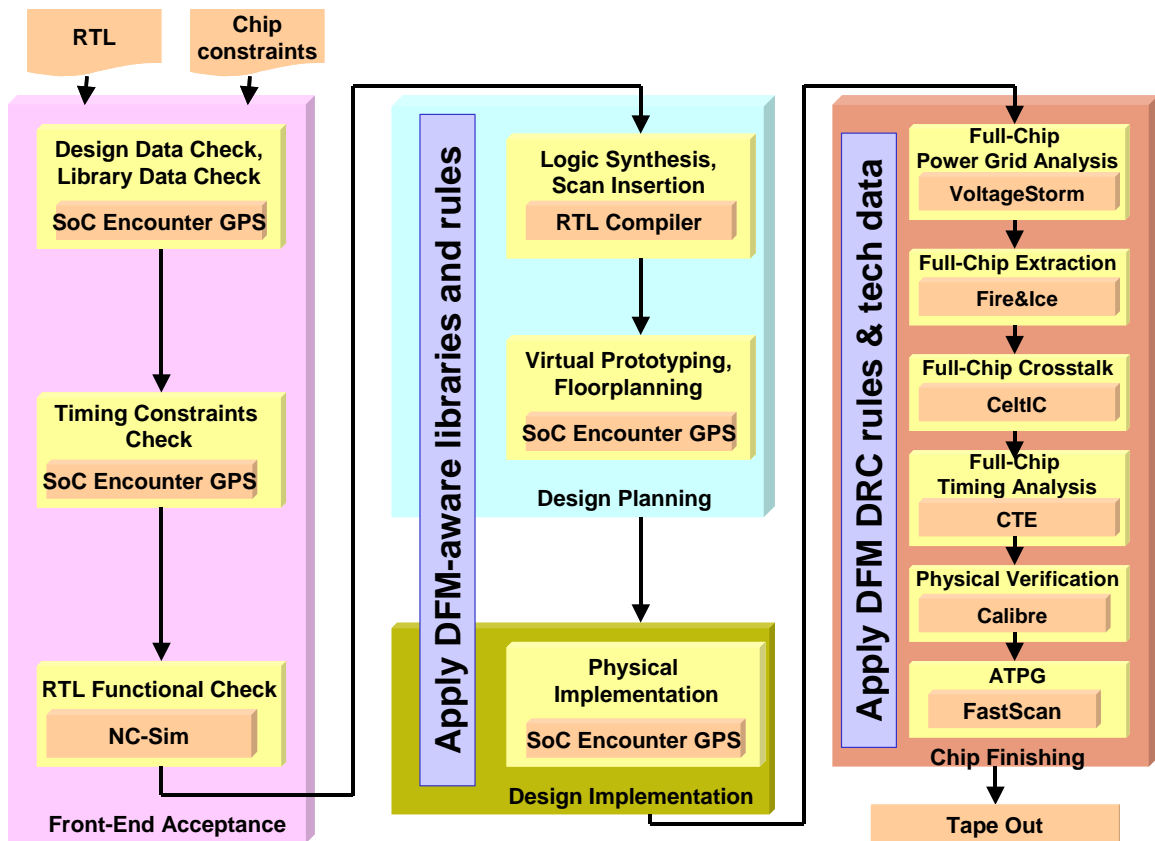


Figure 1. Overview of UMC 90 Nanometer Reference Design Flow