

DATASHEET

UMC - Mentor Graphics 65nm Basic DFT Flow

Today's 65nm electronic IC designs are complex devices and usually contain elements that must work together to make the device function as intended. After the design's functionality is verified and the device is manufactured, it needs to be tested for any defects that may be present. Creating the test program for these devices can be complex as well.

In this reference flow, we use Mentor Graphics' Design-for-Test (DFT) tools to demonstrate a comprehensive DFT solution that can be used in your chip.

This UMC-Mentor Graphics 65nm Basic DFT Reference Flow covers high level information and some basic concept to consider when designers use the DFT tools together on a single design to make sure everything gets tested. All the details for each tool are found in the respective process guides and references manuals. An example design is available to download that includes detailed dofiles and instructions to help you step through a sample DFT procedure of applying DFTAdvisor™, MBISTArchitect™, BSDArchitect™, TestKompres™, and YieldAssist™ to implement a full basic flow DFT test program.

To illustrate the basic DFT flow we will walk through a design example that is mostly digital logic that has a variety of memories spread around the design. The memories should be tested with MBIST in this case. Boundary scan is a requirement for this design and it will control the MBIST controllers that are created to minimize the need for having extra external pins to run the memory tests. ATPG test patterns will be created for both the stuck-at and transition fault models. Since the number of scan channels on the tester is limited, it makes sense to use TestKompres™ to minimize the number of IO pins required for test. Compressed test patterns will run more quickly on the production test floor and require less tester memory. After running the test patterns on the tester, any failure files that are created should be diagnosed to check for any systematic problems that could limit the yield levels.

The basic DFT flow is shown below.

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