FOUNDRY LEADERSHIP FOR THE SoC GENERATION

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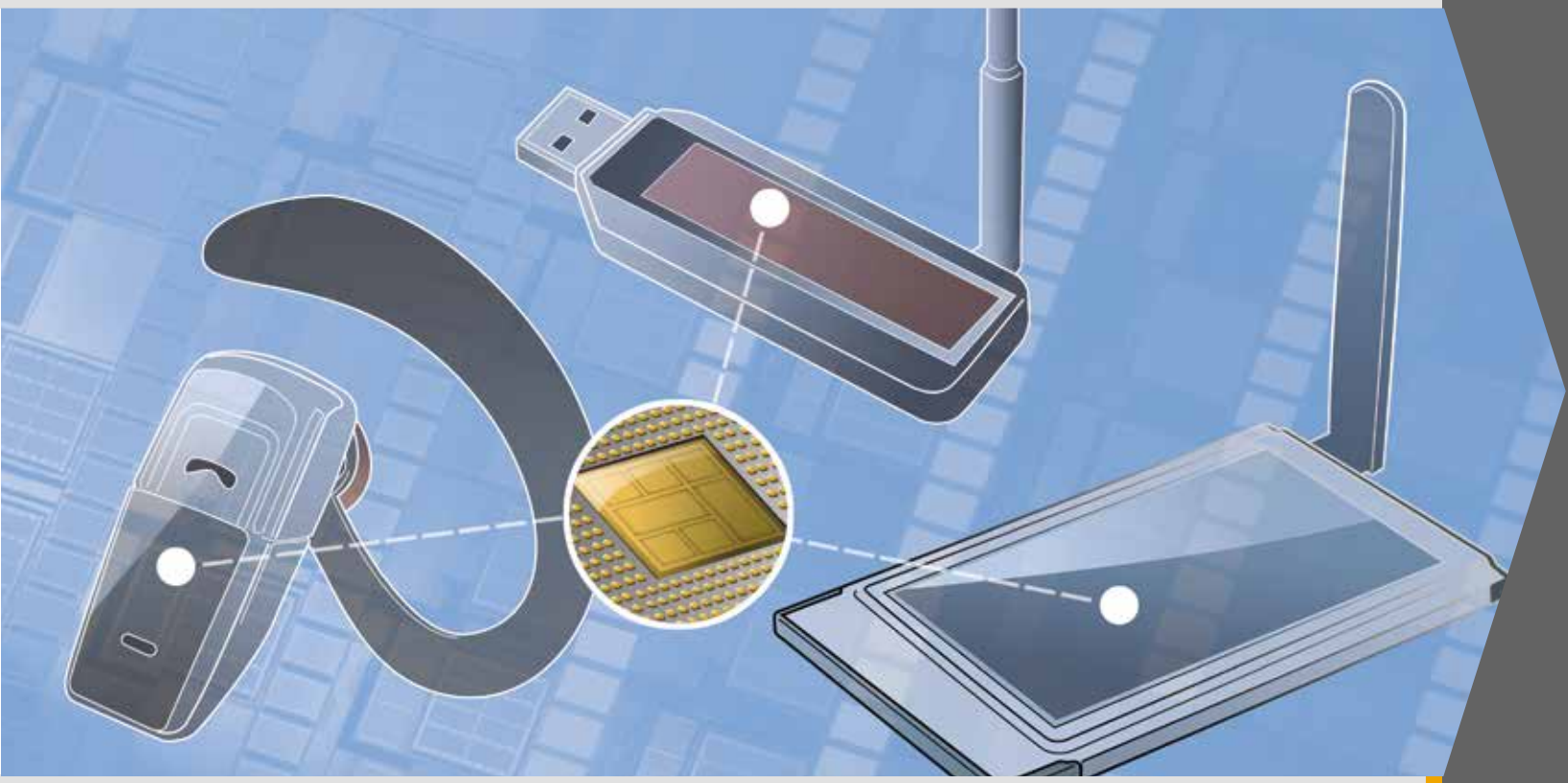
Mixed-Signal/RFCMOS

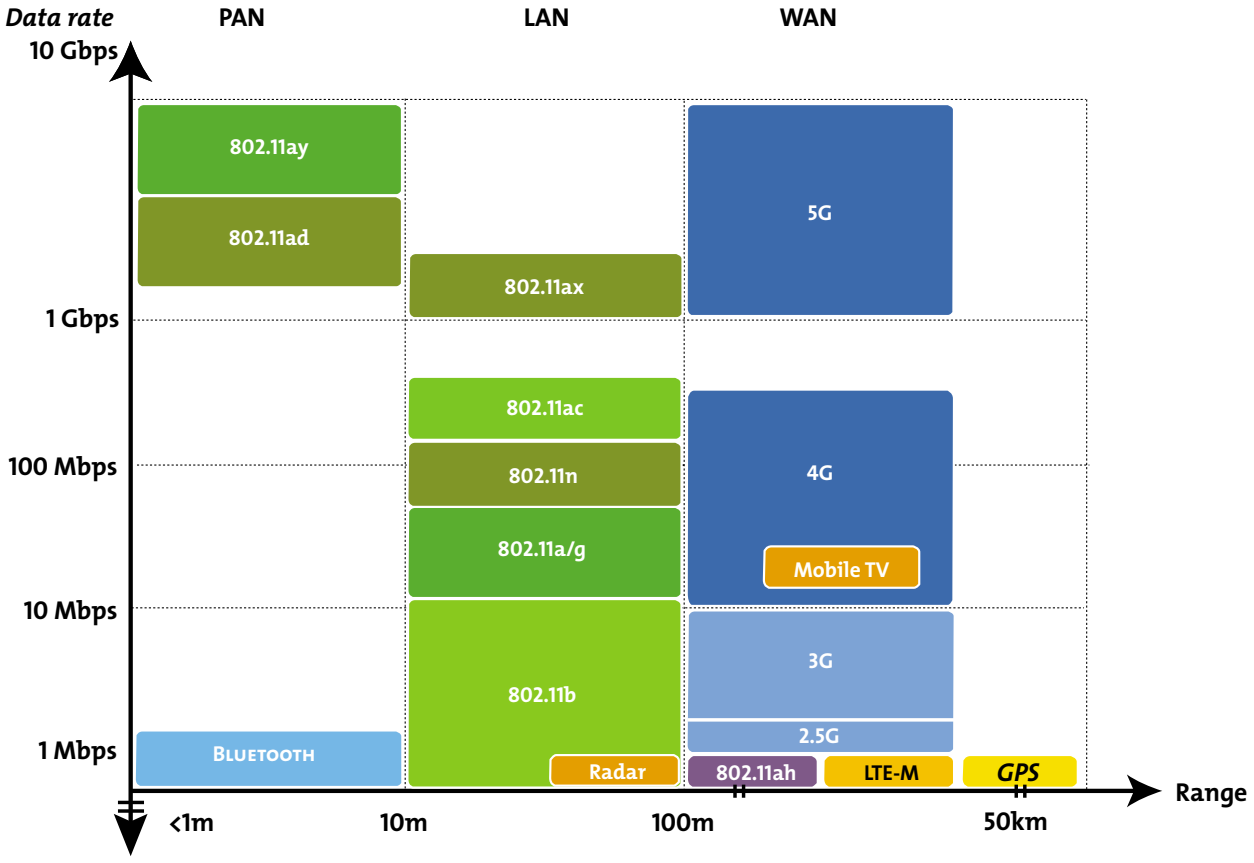


UMC

Solutions for Mixed-Signal/RFCMOS Applications

Mixed-Signal and RFCMOS applications have become major requirements for system-on-chip designs. UMC provides a logic compatible process for Mixed-Signal/RF solutions and offers many advanced features to optimize the passive devices such as inductors and capacitors. The frequency range of UMC's scalable models range up to 20GHz. In addition, UMC works very closely with industry leading EDA vendors to deliver seamless design flows to help accelerate time-to-silicon.

RF/Wireless Landscape



PAN: Personal Area Network, LAN: Local Area Network, WAN: Wide Area Network

Technology and Performance

Technology	250nm	180nm	130/ 110nm	90nm	65/55nm	40nm	28nm	22nm	14nm
GPS	▲	▲	▲	▲	▲	▲	▲	△	△
Cell phone	▲	▲	▲	▲	▲	▲	▲	△	△
Bluetooth	▲	▲	▲	▲	▲	▲	▲	△	△
ZigBee	▲	▲	▲	▲	▲	▲	▲	△	△
Mobile TV	▲	▲	▲	▲	▲	▲	▲	△	△
Wi-Fi	-	▲	▲	▲	▲	▲	▲	△	△
Wi-Fi 802.11n	-	▲	▲	▲	▲	▲	▲	△	△
Wi-Fi 802.11ac	-	-	-	-	▲	▲	▲	△	△
3rd Generation partnership project	-	-	▲	▲	▲	▲	▲	△	△
ADAS Radar	-	-	▲	▲	▲	▲	▲	△	△
Long term evolution	-	-	▲	▲	▲	▲	▲	△	△
5G	-	-	-	-	▲	▲	▲	△	△
IoT/Smart IoT/AIoT	-	-	▲	▲	▲	▲	▲	△	△

△ **Developing**

Key Features

- High Q inductors on the thicker top copper metal
- High density MIM capacitors
- Cost effective Metal Oxide Metal capacitors (MOM)
- Precision poly resistors
- Deep Nwell for noise isolation
- Multiple Vt devices for optimized circuit performance
- Wide tuning range Varactors
- Diodes

Comprehensive MS/RF Platform

UMC's MS/RF technology solutions offer optimum speed and performance. UMC's superior f_T and low NF_{min} satisfy most commercial applications. For portable and consumer applications, UMC provides comprehensive processes in accordance with customers' particular product requirements.

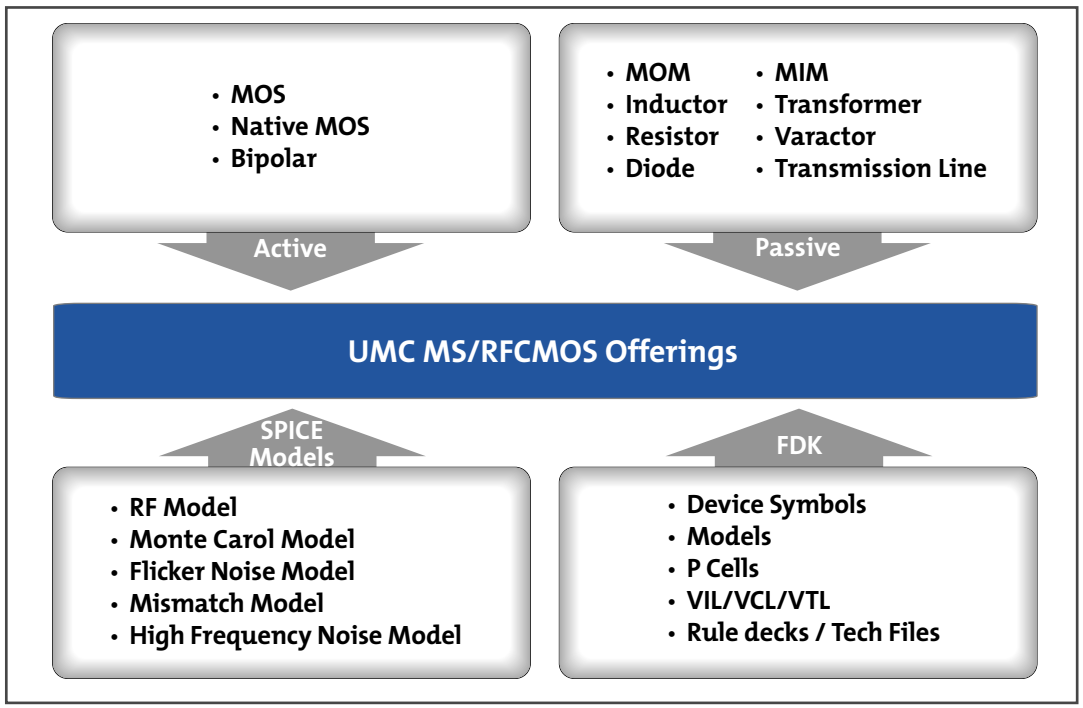
UMC RFCMOS Process Platform

RFCMOS Technology	Process Baselines										
	FFC	HPC^U+	HPC^U	HLP	ULP	ULL	LP	LL	SP	GII	HS
14nm	△	-	-	-	-	-	-	-	-	-	-
22nm	-	-	-		△	△	-	-	-	-	-
28nm	-	▲	▲	▲	-	-	-	-	-	-	-
40nm	-	-	-	-	▲	-	▲	-	-	-	-
55nm	-	-	-	-	▲	-	▲	-	▲	-	-
65nm	-	-	-	-	-	-	▲	▲	▲	-	-
90nm	-	-	-	-	-	-	-	▲	▲	-	-
0.11um*	-	-	-	-	-	-	-	▲	▲	-	▲
0.13um	-	-	-	-	-	-	-	-	-	-	▲
0.18um	-	-	-	-	-	-	-	-	-	▲	-
0.25um	-	-	-	-	-	-	-	-	▲	-	-

FFC: FinFet Compact
HPC^U: High Performance Compact Ultra
HPC^U+: High Performance Compact Ultra Plus
HLP: High Performance Low Power
LP: Low Power
G: Generic
LL: Low Leakage
SP: Standard Performance
HS: High Speed
GII: General Enhance
ULP: Ultra Low Power
GLL: Ultra Low Leakage

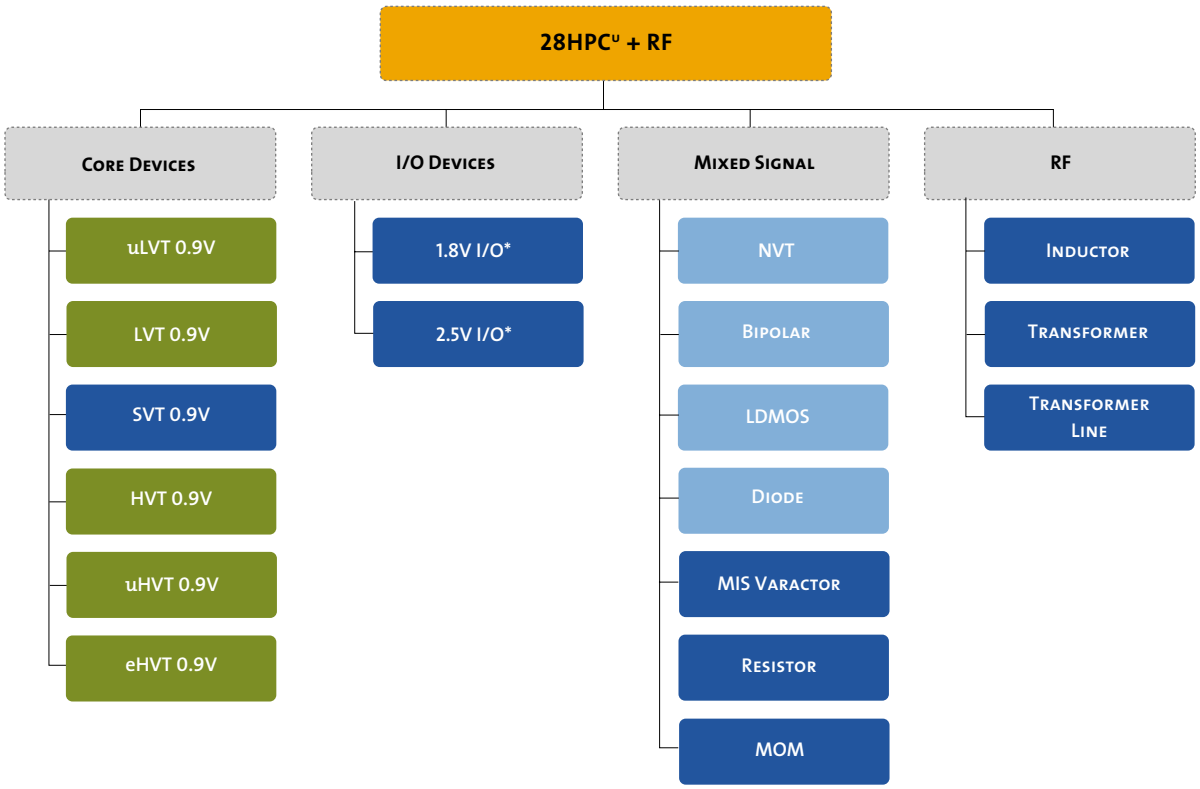
△: Developing
▲: Available
*** : UMC's 0.11um AE process with Aluminum BEOL**

UMC MS/RFCMOS Offerings



Note: VIL/VCL/VTL is Virtual Inductor/Capacitor/Transformer Library
FDK is Foundry Design Kit

28HPC^{U}+ MS/RF Technology Platform



: RF Mode (<30GHz) Support : Mixed Signal Support :mm-Wave Support

* 18V IO: UD 1.5V/1.2V option
** 2.5V IO: OD 3.3V, UD 2.5V/1.8V optione

Active and Passive Devices

Active Devices	L130E	L110AE	90LL	90SP	L65LL	L65LP/SP	L55LP/ULP	40LP/ULP	28HLP	28HPC^{U}	28HPC^{U}+	22ULP	22ULL	14FFC
MOS (Core N,P)	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
MOS (I/O, N,P)	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
Native NMOS	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
BJTs	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
Passive Devices	**L130E**	**L110AE**	**90LL/SP**	**90SP**	**L65LL**	**L65LP/SP**	**L55LP/ULP**	**40LP/ULP**	**28HLP**	**28HPC^{U}**	**28HPC^{U}+**	**22ULP**	**22ULL**	**14FFC**
MOS Varactor	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
Resistors	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
Diodes	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
MIM Capacitor	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
MOM Capacitor	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
Inductors	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
Active Devices	**L130E**	**L110AE**	**90LL**	**90SP**	**L65LL**	**L65LP/SP**	**L55LP/ULP**	**40LP/ULP**	**28HLP**	**28HPC^{U}**	**28HPC^{U}+**	**22ULP**	**22ULL**	**14FFC**
Mismatch Report	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
Characterization Report	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲
Noise Report	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲

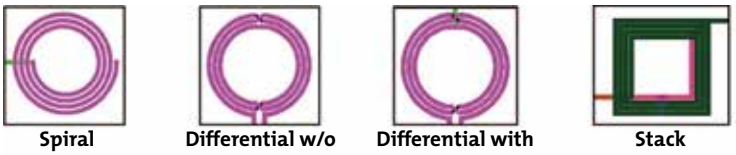
▲ Available

Foundry's First Virtual Inductor/Transformer/Capacitor Libraries

UMC works with its EDA tool partners to deliver the industry's first parameterized design kits. Full wave simulation has been performed on all kits within the Virtual Inductor / Transformer / Capacitor Libraries. The virtual libraries enable RFCMOS designers to create and simulate custom inductor geometries that are based on UMC's processes. These libraries are built upon UMC's Electromagnetic Design Methodology (EMDM), which allows engineers to easily and accurately create any RF structure. EMDM gives designers the flexibility to innovate new geometries simply by editing parameters such as diameter, number of turns or width.

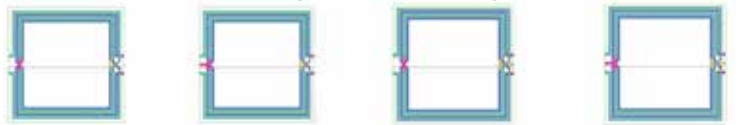
Foundry's First Virtual Library

VIL



Spiral | Differential w/o center tap | Differential with center tap | Stack

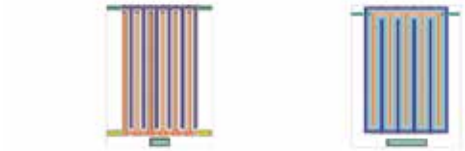
VTL



W/O center tap | CT on primary coil | CT on secondary | CT on both coils | Octagon

- Input: single/differential end
- Output: single/differential end
- Turn Ratio: 1:n, n:2n, n:n

VCL

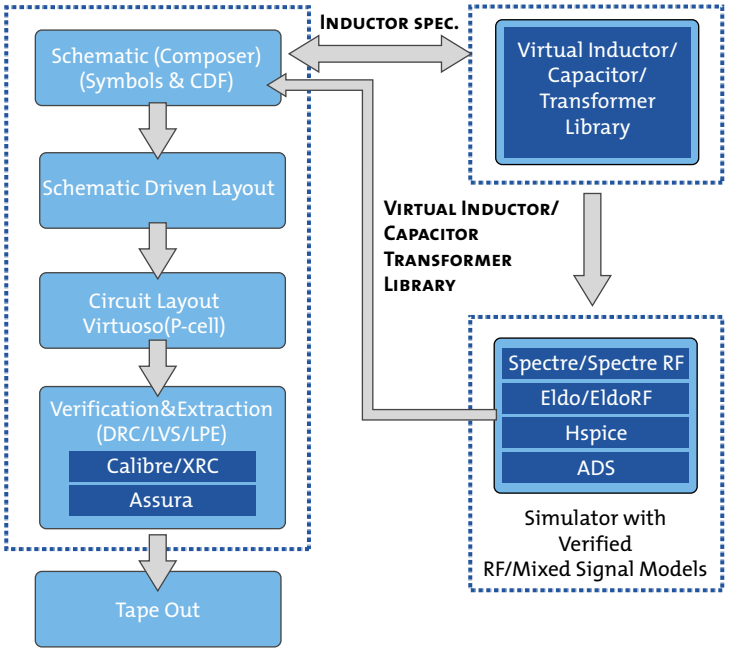


Symmetry | Asymmetry

Note : The Virtual library can be used to simulate all types of RF inductors and capacitors.
CT: Center Tap

MS/RF Design Flow and FDK

The FDK (Foundry Design Kit) provides IC designers with an automatic design environment. The methodology provides access to circuit-level design and simulation, circuit layout, and layout verification using RF device models. In the front-end, fundamental components of UMC's MS/RF process are implemented in common design environments and simulation tools. The back-end includes parameterized cells (P Cell), which includes a schematic driven layout to provide an automatic and complete design flow. Callback functions are also provided in the design flow to minimize data entry. EDA tools for MS/RF designs are also supported.



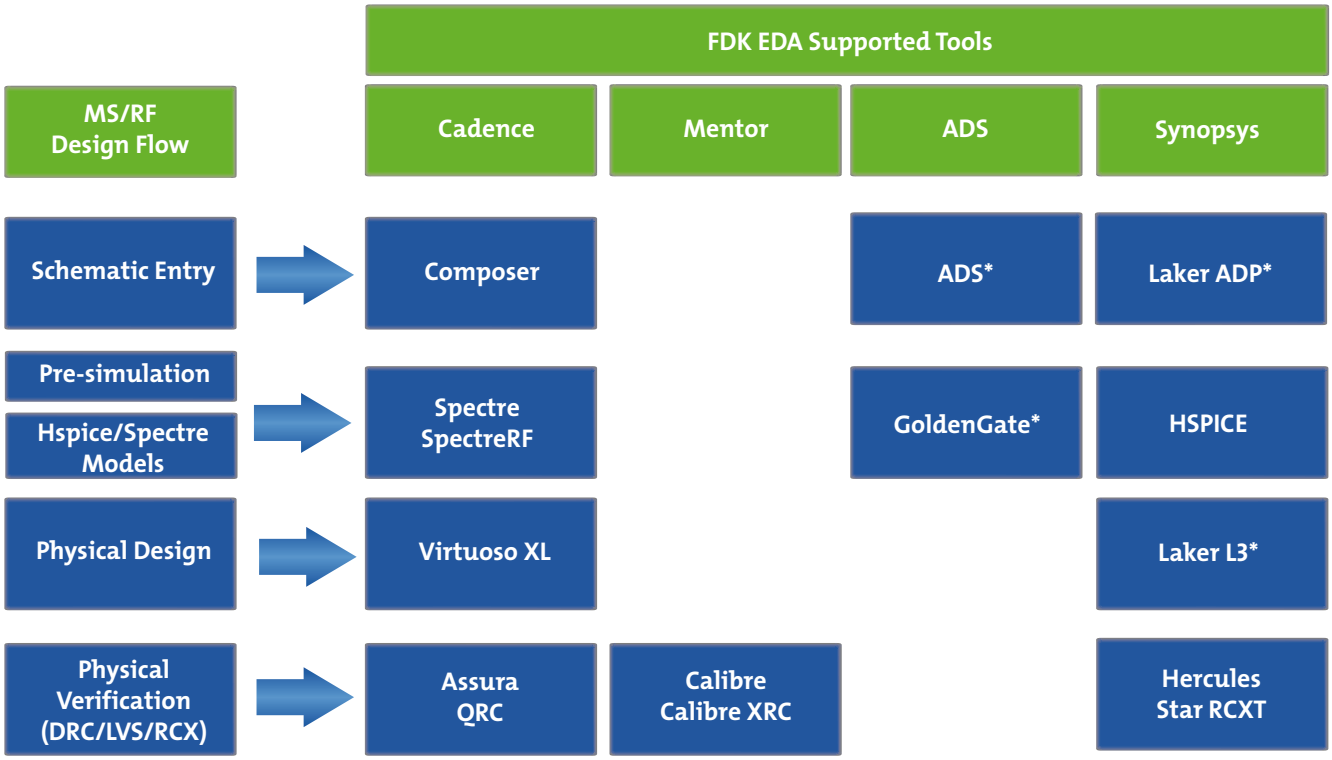
Optimum Inductor/Capacitor/Transformer Finder (OIF/OCF/OTF)

UMC offers the Optimum Inductor Finder (OIF) in the FDK package. The OIF gives designers the ability to quickly access a large library of inductors accurately calibrated to UMC's silicon. It also allows users to perform inductor optimization through just a few simple steps using the user-friendly interface. For instance, customers can define a desired inductor and make trade-offs between Q-factor and area. The OIF will select a design that best fits the specifications in a matter of seconds.

In addition, UMC offers the Optimum Capacitor Finder (OCF) in the FDK package. The OCF gives designers the ability to quickly access a large library of capacitors accurately calibrated to UMC's silicon. It also allows users to perform capacitor optimization through just a few simple steps using the user-friendly interface. For instance, customers can define a desired capacitor and make trade-offs between Q-factor and area. The OCF will select a design that best fits the specifications in a matter of seconds.

UMC also offers the Optimum Transformer Finder (OTF) in the FDK package. The OTF gives designers the ability to quickly access a large library of transformers accurately calibrated to UMC's silicon. It also allows users to perform transformer optimization through just a few simple steps using the user-friendly interface. For instance, customers can define a desired transformer and make trade-offs between impedance and area. The OTF will select a design that best fits the specifications in a matter of seconds.

FDK EDA Supported Tools



Note: *is available by request

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