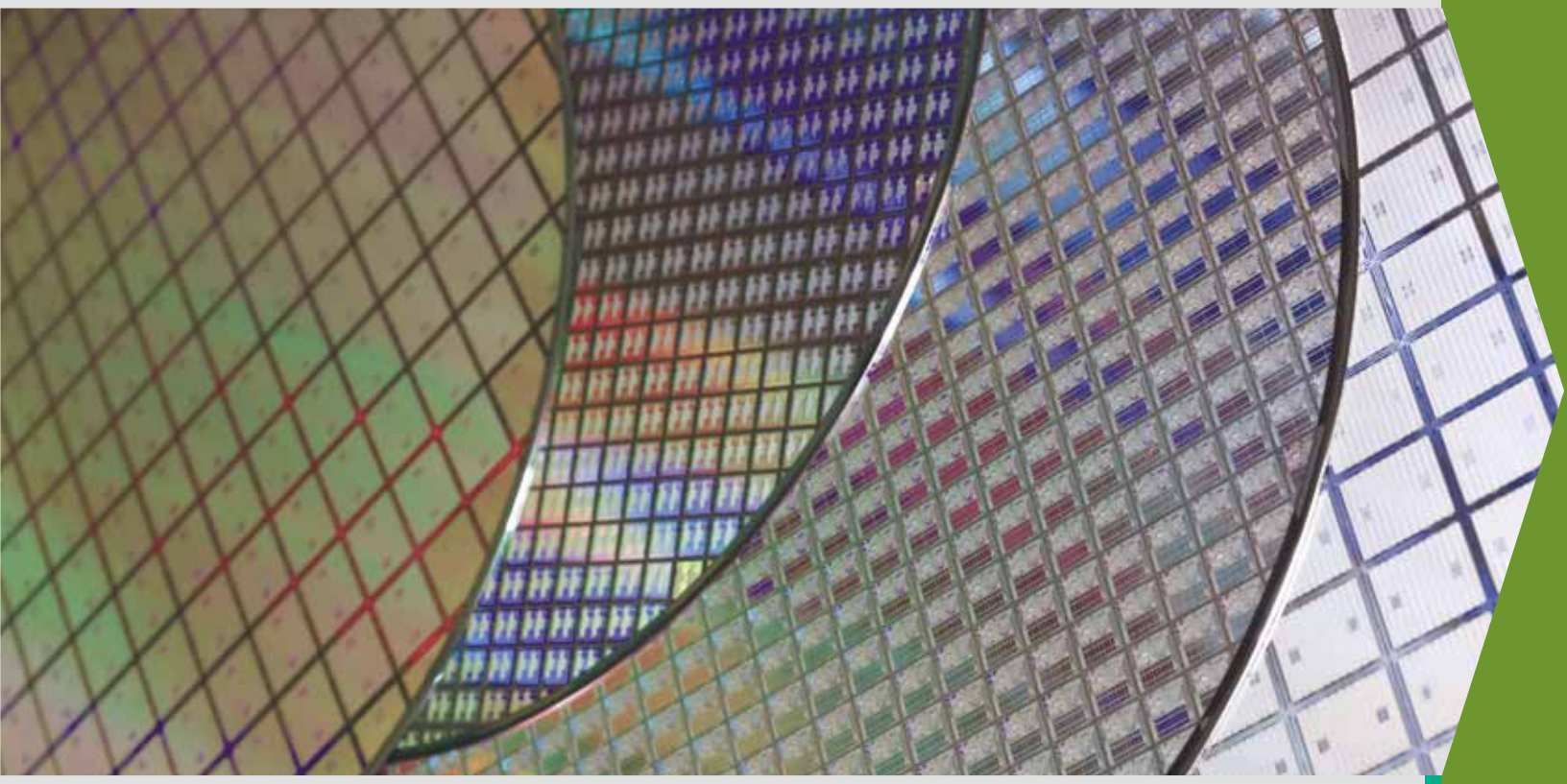
40 Nanometer

40



UMC

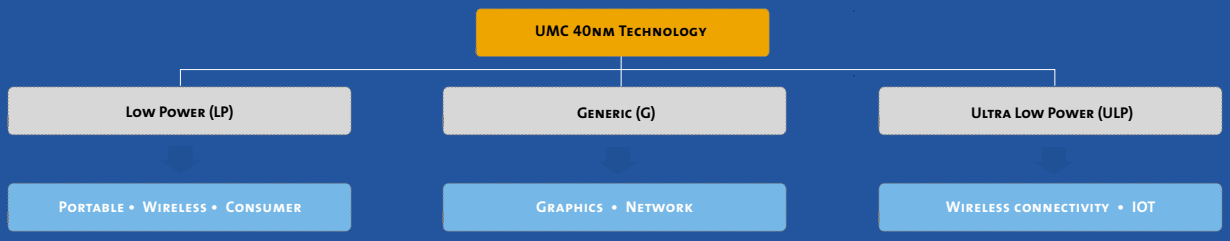
40 Nanometer

UMC's volume production 40-nanometer technology supports today's high performance and low power requirements. Many customers have engaged with UMC for their 40nm projects, with multiple designs in various stages of production. UMC's 40nm utilizes advanced processes such as immersion lithography, ultra shallow junction, mobility enhancement techniques and ultra low-k dielectrics for maximum power and performance optimization. UMC's 40nm process consists of a low power platform (LP) focusing on the low power and low leakage design requirements for mobile and consumer applications, and a generic platform (G) that is optimized for a broad range of consumer and high-speed applications. Designers also benefit from comprehensive device offerings that include features to help optimize power and performance, different I/O voltage choices and analog/RF design resources.

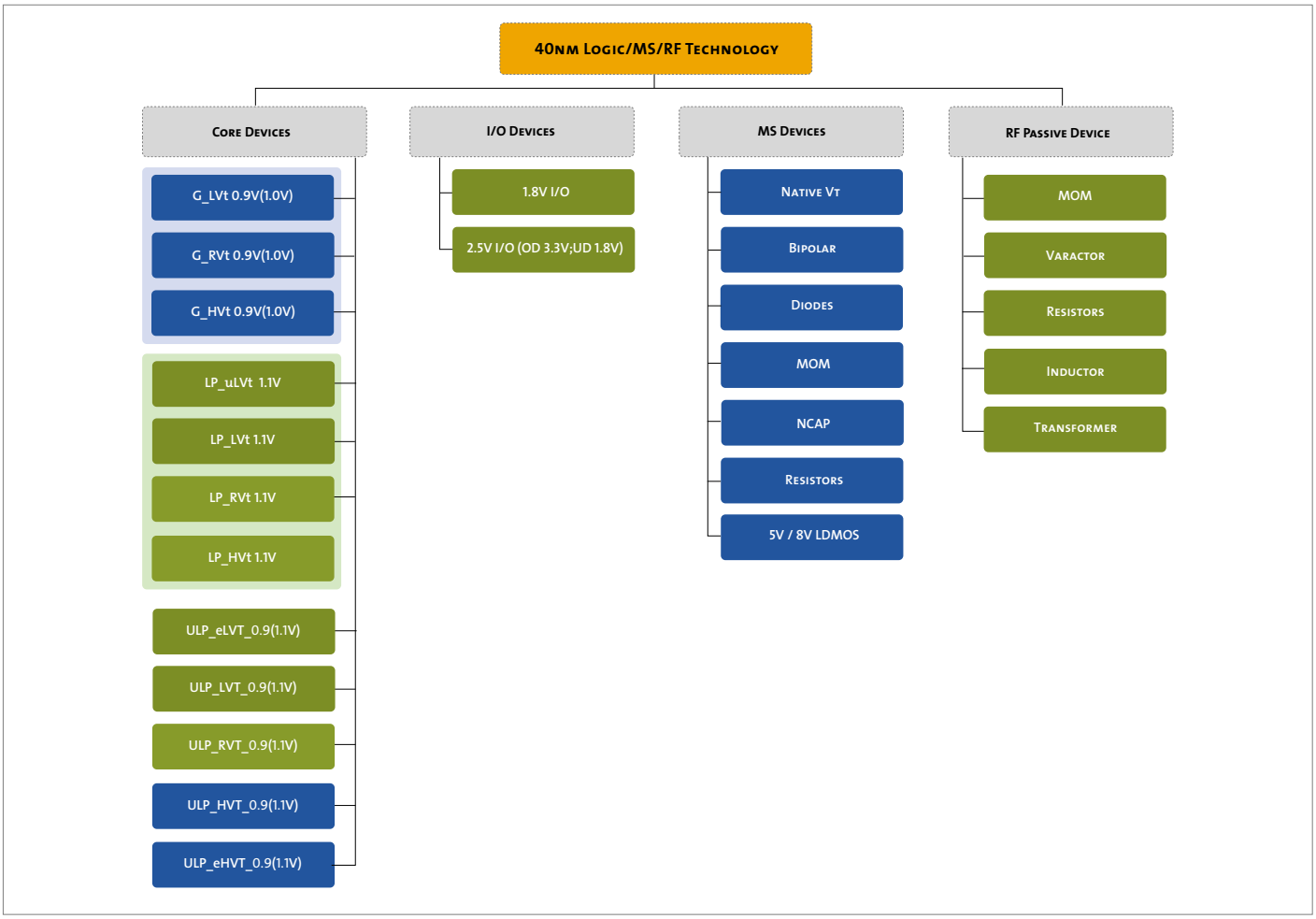
40nm Key Features

- *Lower operating voltage down to 0.9V ultra low leaage device*
- *Integrated flows for logic, Mixed-Signal/RF*
- *Shallow trench isolation*
- *Retrograde twin well (Triple well option)*
- *Immersion Lithography implemented by NA=1.2*
- *Mini-second anneal technology for ultra shallow junction*
- *Poly gate & S/D with NiSi process*
- *Advanced mobility enhancement techniques (Channel orientation, SMT, DSL, eSiGe)*
- *Up to 1P11M copper metal layers with ULK (k=2.5)*
- *6T/8T SRAM bit cell option*
- *e-Fuse option*
- *BOAC (Bonding Over Active Circuit)*
- *Wire Bond/Flip Chip option*

Technology to Meet Broad Applications



40nm Logic/MS/RF Devices



G: Generic Platform LP: Low Power ■: RF model available; other models available upon customer request

Comprehensive IP Portfolio

UMC offers comprehensive design resources that enable our customers to fully realize the advantages of UMC's advanced technologies. UMC's fundamental IPs (standard cells, I/Os, and memory compilers) help customers easily migrate their designs to the next process generation to realize significant performance advantages while also reducing die size. UMC has collaborated with RF IP company to offer competitive solutions.

Customers can also leverage application specific IPs that are specialized for all types of mainstream applications such as digital TVs, cellular baseband controllers, graphics, and networking Bluetooth, WiFI, GPS application to overcome time-to-market challenges.

DTV

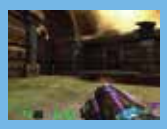
PLL, USB, LVDS, Embedded Memory, HDMI, DDRn

Baseband

Mobile DDR,USB, LVDS, PLL, Embedded Memory

Graphic

DDRn, PCI-e, HDMI, LVDS, Embedded Memory



Networking

Mobile DDR, USB, PCI-e, SATA, Embedded Memory

Fundamental IP Support

Fundamental IPs (standard cells, I/Os, and memory compilers listed below) are optimized to UMC technologies, and are planned for development from several leading vendors to be available free-of-charge (please contact a UMC account manager for more information). Customers can also leverage application specific IPs for DTV, graphics, networking, etc. IPs available through UMC are DFM (Design for Manufacturing) compliant for better manufacturability.

Process Node		40nm LP	40nm uLP
Standard Cell Library	eLVT	-	√
	LVT	√	√
	RVT	√	√
	HVT	√	√
	eHVT	-	√
I/O Library	1.8V	√	√
	1.8V_UD1.5V	√	√
	2.5V	√	√
	2.5V_OD3.3V_UD1.8V	√	√
eFuse	32b ~ 4Kb	√	√
Single Port SRAM Compiler		√	√
Dual Port SRAM Compiler		√	-
Single Port Register File		√	√
Dual Port Register File		√	-
ROM Compiler		√	√

Interface/Functional IP Support

ITEM	Feature	Vendor	40nm LP	40nm uLP
USB 2.0	pico PHY	Synopsys	√	√
USB 3.0	5Gbps	Synopsys	√	√
PCIE	Gen II	Synopsys	√	√
SATA3	6G	Synopsys	√	√
DDR multi PHY	DDR2, 3, 3L, mDDR, LPDDR2 PHY(1066)	Synopsys	√	√
DDR 3/2	1600MHz	Synopsys	√	√
HDMI	1.4a TX & HEAC	Synopsys	√	√
MIPI D PHY	TX & RX	Synopsys	√	√
PLL	Input frequency range:25~66MHz, Output frequency range:200~400MHz	FTC	√	√
PLL	Input frequency range:20~200MHz, Output frequency range:500~ 1000MHz	FTC	√	√
OTP	8Kb~4Mb	Kilopass	√	√

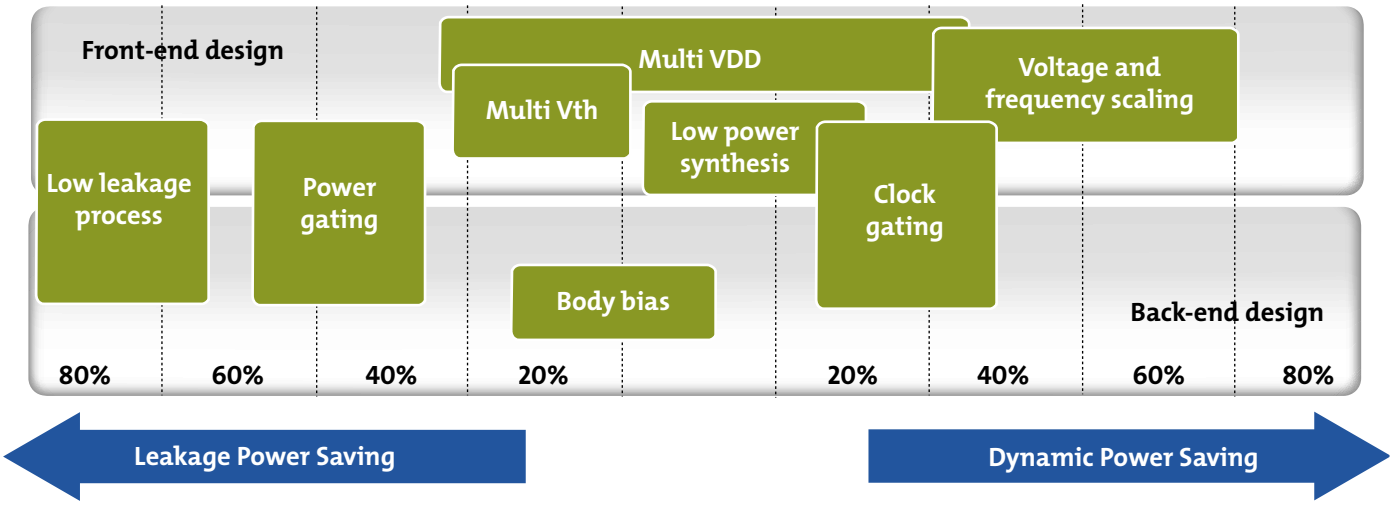
*For more information, please contact your account manager.

Low Power Features of Standard Cell Library

With today's proliferation of low power applications, lowering energy consumption without sacrificing performance has become a critical concern for designers of power management chips for portable electronics. UMC supports its standard cell library with low power design features, including multiple Vt, clock-gating, level shifter and other features to complement UMC's complete low power solution.

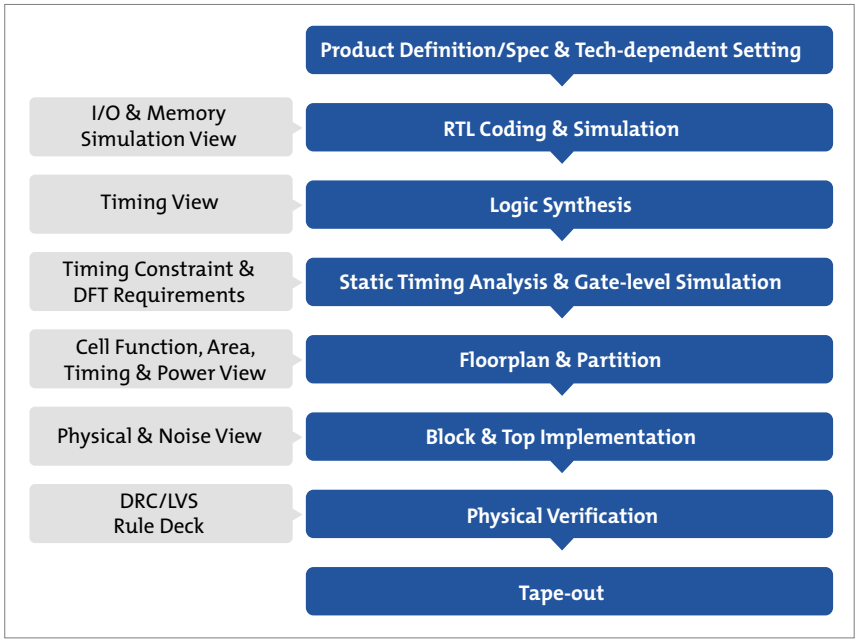
Type		Support Features		Support				
				28nm	40nm	65nm	90nm	0.13um
Operating Power	Voltage Island & Scaling	Level Shifters w / Insulator	Power & Timing Model @ 80% of Vdd	√	√	√	√	√
	Clock Gating & Frequency Scaling	Clock Gated F/F		√	√	√	√	√
Leakage Power	Multi-Vt	Multi-Vt cells		√	√	√	√	√
	Power Gating	Isolation cells, Retention F/F Headers / Footers, etc.		√	√	√	√	√
	Body Bias	Tapless cells	Timing / Power Model	√	√	√	√	√

Low Power Design Support



UMC Reference Design Flow

UMC Reference Design Flow provides a design methodology and flow validated with a "Leon2" system demonstration board. The flow incorporates 3rd-party EDA vendors' baseline design flows to address issues such as timing closure, signal integrity, leakage power and design for manufacturability and adopts a hierarchical design approach built upon silicon validated process libraries. UMC Reference Design Flow covers from RTL coding all the way to GDS-II generation and supports Cadence, Magma, Mentor and Synopsys EDA tools. All of these tools can be interchanged for added flexibility.



SYNOPSYS®

Mentor Graphics®

cadence®

Reference Design Flow and Vendor Support

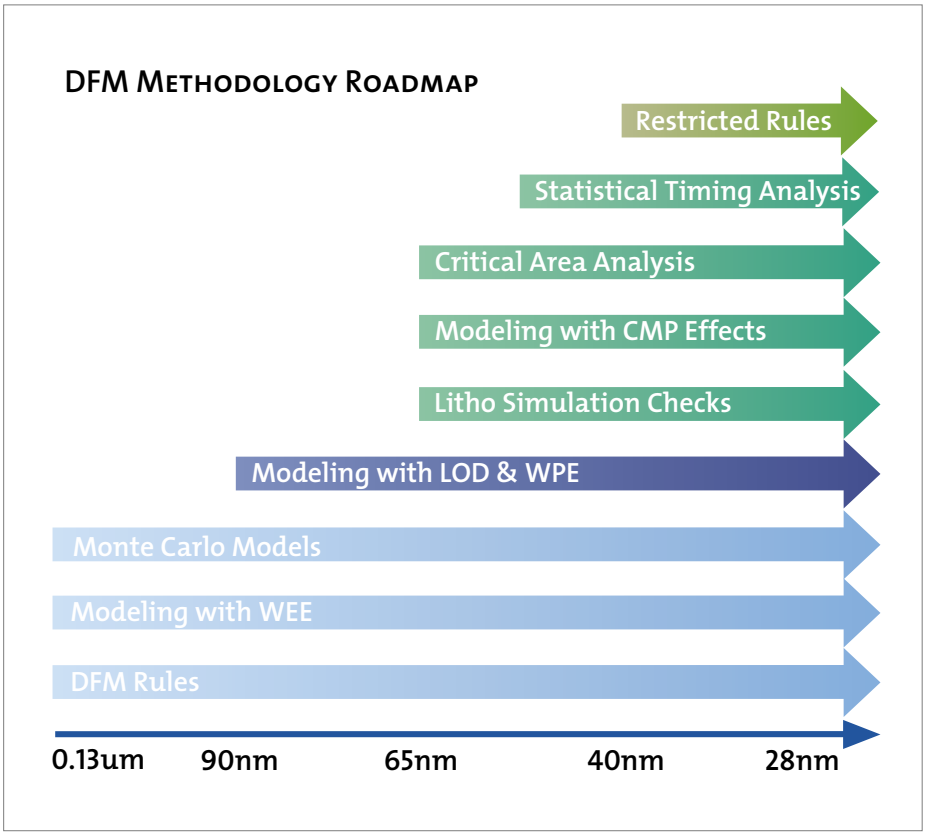
UMC works with leading EDA tool companies to provide a verified Reference Design Flow program to ensure the accuracy of customer designs in a proven environment. UMC's Reference Design Flow program integrates solutions for digital designs and low power solutions that incorporate the latest DFM resources available from leading third-party providers. Tools can be interchanged for added flexibility.

Features of Design Flow	Cadence	Synopsys	Mentor
Functional Logic Simulation	▲	▲	▲
Schematic Entry	▲	▲	-
Logic Synthesis	▲	▲	-
Static Timing Analysis	▲	▲	-
Timing Closure	▲	▲	-
Signal Integrity	▲	▲	-
Floor Planning	▲	▲	-
Physical Synthesis	▲	▲	-
Multi-Vt Low Power	▲	▲	-
Multi-Vdd Low Power	▲	▲	-
Design For Test	▲	▲	▲
Design For Diagnosis	▲	▲	▲
DFM - double via insertion	▲	▲	▲
DFM - dummy metal filling	▲	▲	▲
Circuits Simulation	▲	▲	▲
Power Analysis	▲	▲	-
Layout Editor	▲	▲	▲
Place & Route	▲	▲	-
Physical Verification	▲	▲	▲
Formal Verification	▲	▲	-
Parasitic Extraction	▲	▲	▲
Noise Analysis	▲	▲	-

Note: ▲ Available

DFM Methodology

UMC offers optimal DFM (Design For Manufacturability) solutions to effectively and efficiently address factors that may negatively affect yield and performance for advanced technology designs. UMC's DFM solutions include advanced process models incorporated in SPICE and extraction decks for predicting random and systematic variations, technology files, DFM-compliant libraries and IP that embrace the intricacies of the fabrication process. Concise DFM recommendation rules are available along with a comprehensive rule-deck runset strategy to fulfill various design requirements.



UMC also offers pre-tapeout Optical Proximity Correction (OPC) and Litho Rule Check (LRC) for custom designs in addition to our standard post-tapeout services that include OPC, Litho Simulation Check (LSC), dummy fill, and metal slotting. At 65nm and below, UMC offers a DFM Design Enablement Kit (DEK) to seamlessly support model-based DFM tools. The DEK has a built-in Graphic User Interface (GUI) for DFM design database setup, and is completed with application notes and qualification reports for design reference.

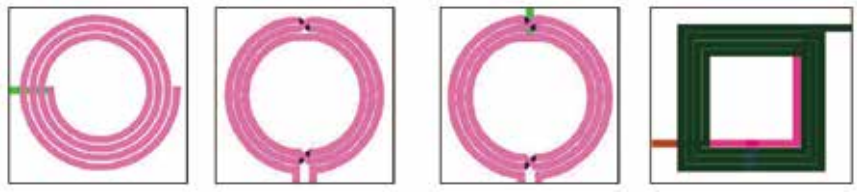
UMC e-Fuse Features

To reduce chip area, achieve better reliability performance, and shorten repair time compared to conventional Al fuse, UMC has developed an e-fuse solution to target the needs of a broad range of applications. The fuse array and complete functional macro are offered to ease the integration process for customers. Both wafer level and package level fuse are supported. Moreover, customers can use e-fuse for the OTP (one time programming) function to save overall costs.

Logic Compatible	• No extra masks necessary • Only one extra pad required
Complete Functional IP Macros	• Fuse array, programming circuit, sensing amplifier • Serial and parallel architecture
Design-Friendly Features	• Allows metal routing over fuses (M6 and above) • Programmable at package level
Flexibility	• Wafer level fuse options • Package level fuse options

Virtual Inductor Library

UMC has worked with its EDA tool partners to deliver the industry's first parameterized inductor design kit based on full-wave simulation: the Virtual Inductor Library (VIL). The VIL enables RFCMOS designers to create and simulate custom inductor geometries that are compatible with UMC's processes. It is built upon UMC's Electromagnetic Design Methodology (EMDM), which allows engineers to easily and accurately create any RF structure. EMDM gives designers the flexibility to innovate new geometries simply by editing parameters such as diameter, number of turns or width.

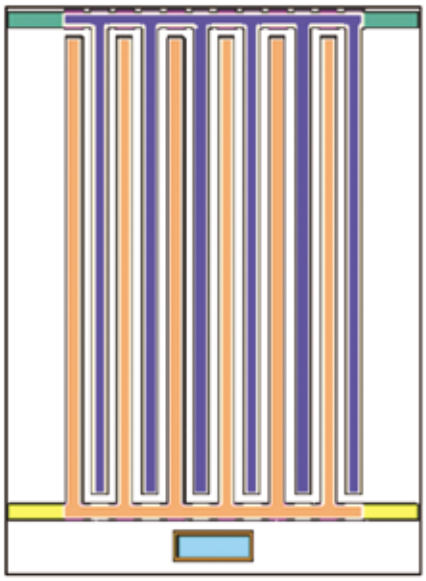


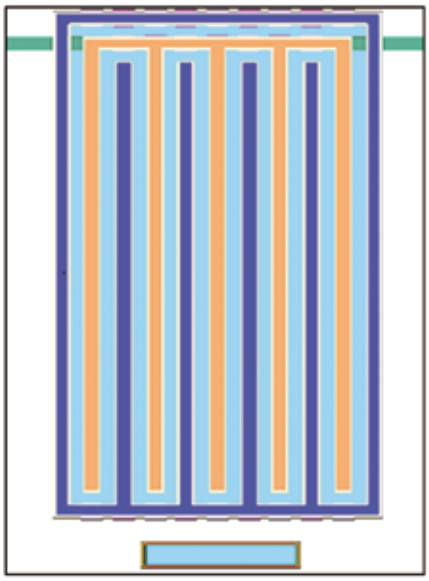
Spiral | Differential w/o center tap | Differential with center tap | Stack

The GUI based VIL can be used to simulate all types of RF inductors.

Virtual Capacitor Library

UMC and its EDA tool partners have delivered the industry's first parameterized MOM capacitor design kit based on full-wave simulation: the Virtual Capacitor Library (VCL). The VCL enables RFCMOS designers to create and simulate custom capacitor geometries that are compatible with UMC's processes. It is built upon UMC's Electromagnetic Design Methodology (EMDM), which allows engineers to easily and accurately create any RF structure. EMDM gives designers the flexibility to innovate new geometries simply by editing parameters such as number of metal and fingers, arrays, and length of fingers for capacitor.

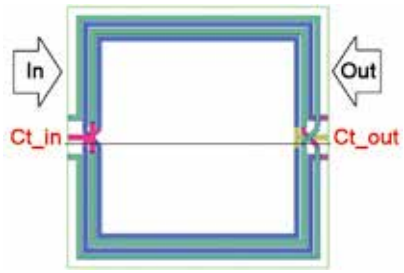




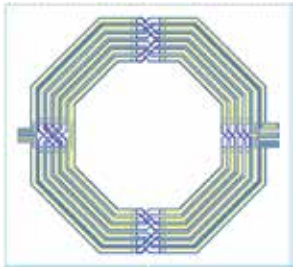
The GUI based VCL can be used to simulate all types of RF capacitors.

Virtual Transformer Library

UMC has also worked with its EDA tool partners to deliver the industry's first parameterized transformer design kit based on full-wave simulation: the Virtual Transformer Library (VTL). The VTL enables RFCMOS designers to create and simulate custom transformer geometries that are compatible with UMC's processes. It is built upon UMC's Electromagnetic Design Methodology (EMDM), which allows engineers to easily and accurately create any RF structure. EMDM gives designers the flexibility to innovate new geometries simply by editing parameters such as primary impedance, secondary impedance, number of turns, mode, and frequency for transformer.



Square



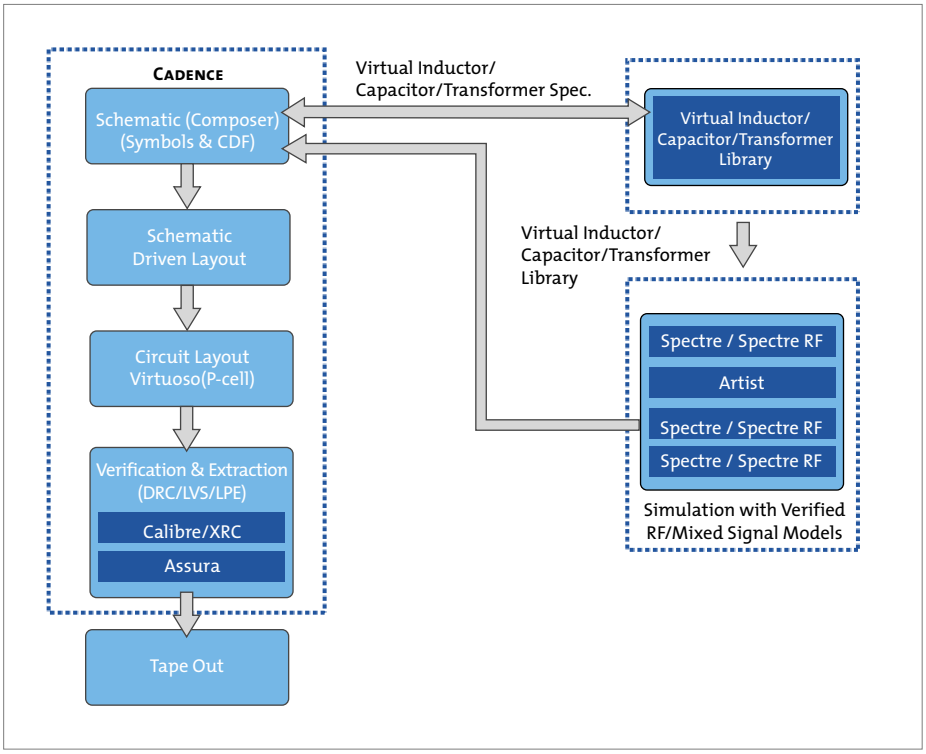
Octagon

- **Input: single/differential end**
- **Output: single/differential end**
- **Turn Ratio: 1:n, n:2n, n:n**

The GUI based VTL can be used to simulate all types of RF transformers.

MS/RF Design Flow and FDK

The FDK (Foundry Design Kit) provides IC designers with an automatic design environment. The methodology provides access to circuit-level design and simulation, circuit layout, and layout verification with accurate RF device models. In the front-end, fundamental components of UMC's MS/RF process are implemented in common design environments and simulation tools. The back-end includes parameterized cells (P Cell), which include a schematic driven layout to provide an automatic and complete design flow. Callback functions are also provided in the design flow to minimize data entry. EDA tools for MS/RF designs are also supported.



Optimum Inductor Finder (OIF)

UMC offers the Optimum Inductor Finder (OIF) in the FDK package. The OIF gives designers the ability to quickly access a large library of inductors calibrated to UMC's silicon. It also allows users to perform inductor optimization through just a few simple steps with the user-friendly interface. For instance, customers can define a desired inductor and make trade-offs between Q-factor and area. The OIF will select a design that best fits the specifications in a matter of seconds.

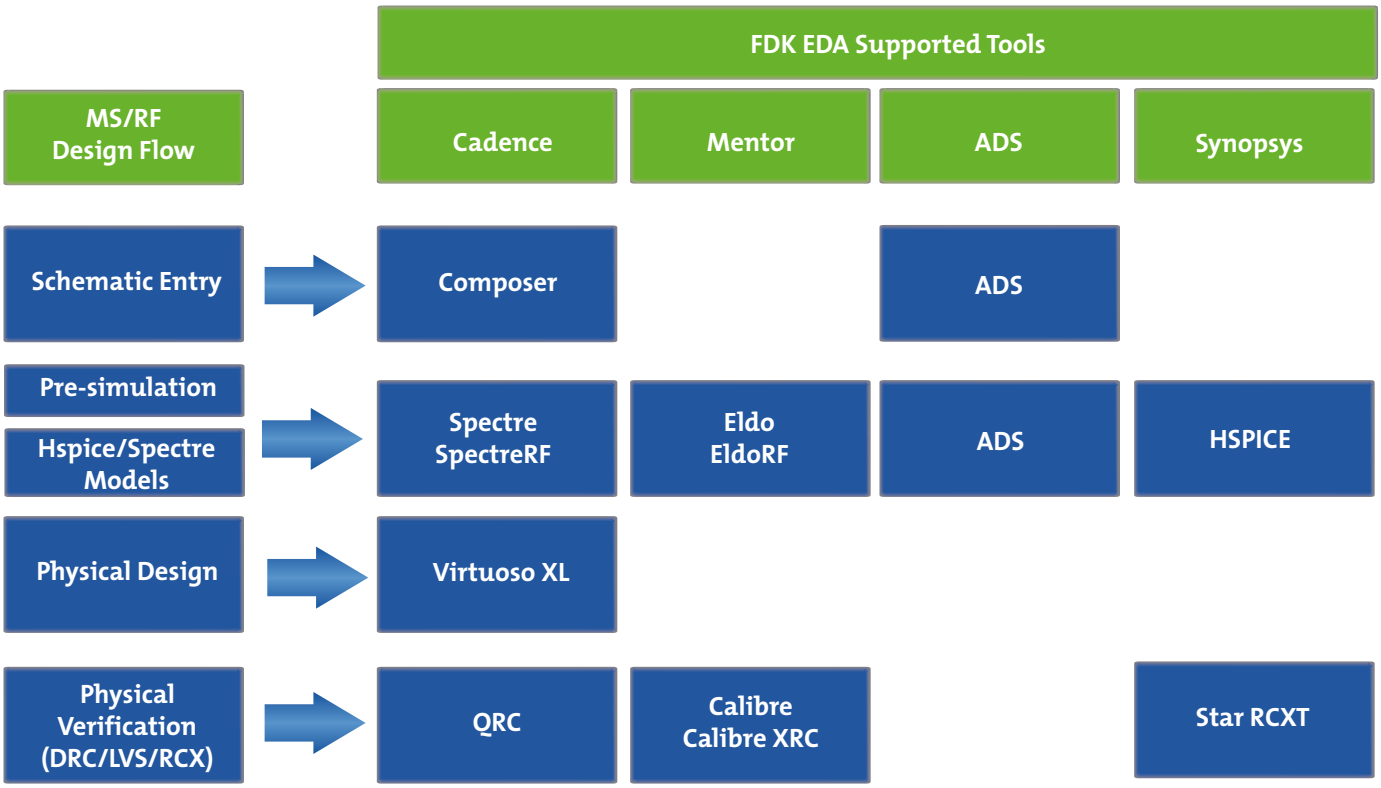
Optimum Capacitor Finder (OCF)

UMC offers the Optimum Capacitor Finder (OCF) in the FDK package. The OCF gives designers the ability to quickly access a large library of capacitors calibrated to UMC's silicon. It also allows users to perform capacitor optimization through just a few simple steps with the user-friendly interface. For instance, customers can define a desired capacitor and make trade-offs between Q-factor and area. The OCF will select a design that best fits the specifications in a matter of seconds.

Optimum Transformer Finder (OTF)

UMC offers the Optimum Transformer Finder (OTF) in the FDK package. The OTF gives designers the ability to quickly access a large library of transformers calibrated to UMC's silicon. It also allows users to perform transformer optimization through just a few simple steps with the user-friendly interface. For instance, customers can define a desired transformer and make trade-offs between impedance and area. The OTF will select a design that best fits the specifications in a matter of seconds.

Analog Design Methodology



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