

## DATASHEET

# UMC Cadence Low Power CPF Reference Flow

The UMC low power CPF reference flow provides a top-down solution from RTL to GDSII using tools from Cadence and Mentor Graphics. Furnished with a comprehensive arsenal of EDA tool scripts and flow steps, this hierarchical flow not only resolves phenomenon encountered with UMC's 65nm process, but also prepares designers for potential issues that might arise from low power design strategies. Besides, DFY and CAA features are also explored in the flow. As such, this low power CPF flow is intended to adapt to any customer design environment by using the highly flexible and configurable LEON-2 processor as its core to exercise its flow steps. It also offers a robust means to help increase our customers' SoC design competitiveness by accelerating their time-to-silicon and avoiding pricey re-spins. This design flow is segmented into four comprehensible phases: Design Acceptance, Design Planning, Design Implementation, and Chip Finishing.

In modern technologies of low power digital design methodology, the power intent for the full chip can be effectively captured using the Common Power Format (CPF). The CPF file serves as a single specification that captures power intent throughout the flow-design, verification and implementation. It also contains library and other technology specific information used for synthesis and implementation. For detailed information and specification about CPF, it can be reached via the website <http://www.si2.org>.

### Phase 1: Design Acceptance

Prior to venturing into the design flow, rigorous checks are meticulously performed on the design & library data, timing constraints, and the intended RTL functions.

### Phase 2: Design Planning

In this stage, the Top-Down low power CPF aware synthesis is done. Scan chains are inserted to provide easy access to internal nodes. Then power domain is created to effectively manage the power information of cell libraries. Meanwhile, the isolation cells are inserted to the net connected the cells within the different power domains.

### Phase 3: Design Implementation

In this stage, physical implementation is performed with timing closure and low power consumption. Power gating cells are automatically handled and arranged in this phase. A sequence of actions is then conducted to complete time-driven placement, scan chain reordering, time-driven routing, RC extraction, clock tree synthesis, in-place optimization, filler cell insertion, SI prevention, and cross-talk analysis are some of the steps.

**Phase 4: Chip Finishing**

The final stage refines the full chip implementation to achieve final timing closure. Full-chip extraction, final timing analysis, power and IR-drop analysis, and physical verification are performed. Before the tapeout-ready GDS file was ready, DFY and CAA methodologies were adopted to ensure the quality of physical design.

# UMC Cadence Low Power CPF Reference Flow

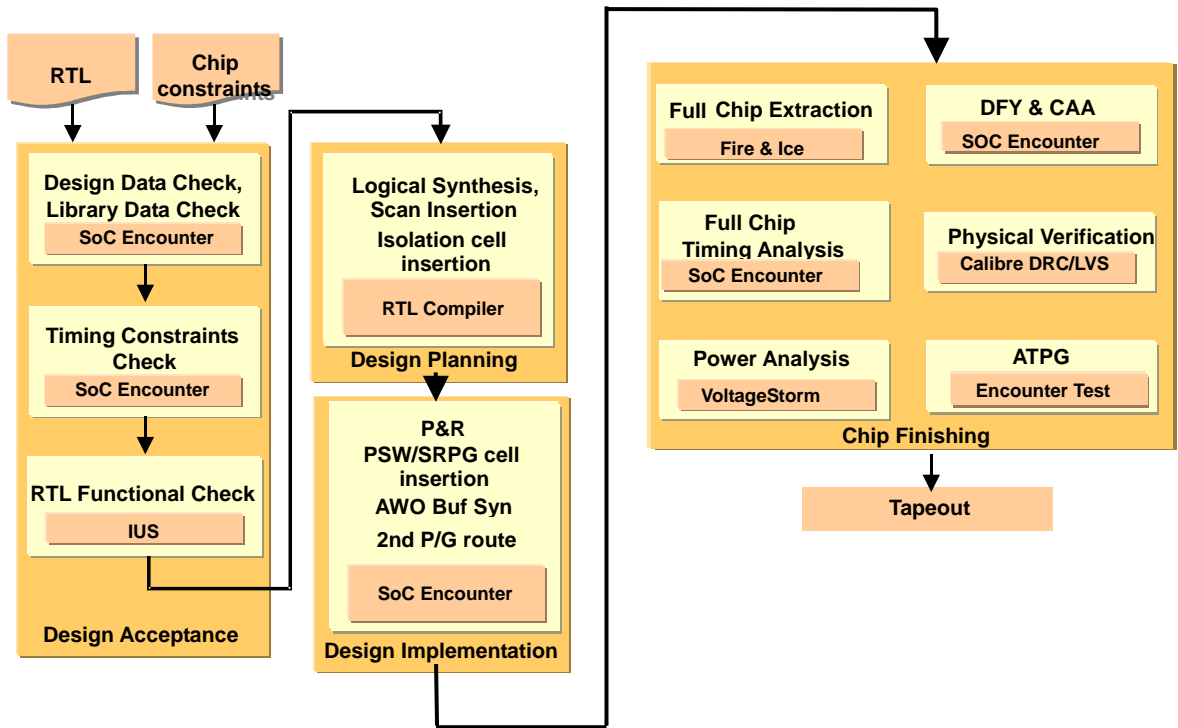


Figure 1. Overview of UMC Cadence Low Power CPF Reference Flow