

## DATASHEET

# UMC-Magma 65LL Low Power UPF Reference Flow

The UMC-Magma Low Power UPF Reference Flow provides a top-down solution from RTL to GDSII in the Talus power platform, which fully supports the industry leading standard Unified Power Format (UPF).

This hierarchical flow not only resolves phenomenon encountered with UMC's 65nm process and IPs, but also eliminates many potential issues that may arise from low-power design strategies.

As such, this low power UPF flow is intended to adapt to any customer design environment by using the highly flexible and configurable LEON-2 processor as its core to exercise its flow steps.

It also offers a robust means to help increase our customers' SoC design competitiveness by accelerating their time-to-silicon and avoiding pricey re-spins. This design flow is segmented into three comprehensible phases with UPF: Synthesis, Layout and Sign-off.

### Phase 1: Synthesis

In this stage, Fix rtl command performs RTL optimization on an elaborated RTL design and generates a technology-independent implementation using Magma primitive cells. Fix netlist command converts an RTL design previously processed by the *fix rtl* command into a netlist of Hypercell models.

### Phase 2: Layout

In this stage, Create floorplans and attach module cells to domains. Power switch cells are automatically handled and arranged in this phase. A sequence of actions is then conducted to complete time-driven placement, scan chain reordering, clock tree synthesis, time-driven routing and post-route optimization.

### Phase 3: Sign-off

The final stage refines the full chip implementation to achieve timing/power analysis, multi-voltage rule checking, formal checking and function verification. Finally the tapeout-ready GDS file will be ready.

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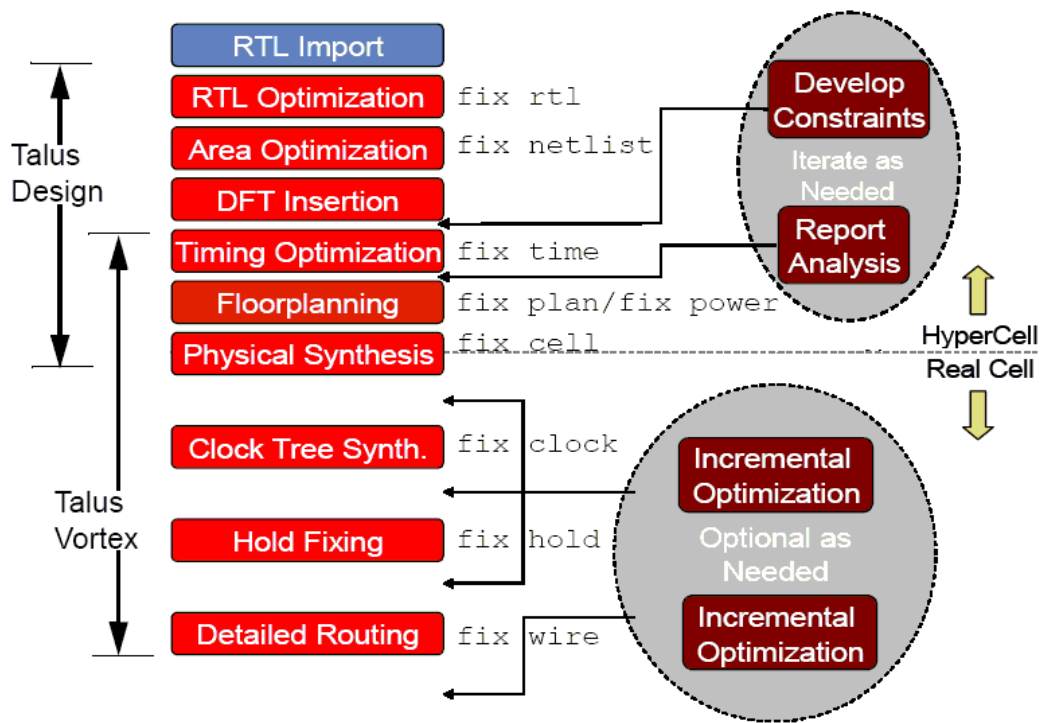


Figure 1. Overview of UMC-Magma Low Power UPF Reference Flow