

## Notice in Usage of This Reference Flow

Dear Valued Customer,

Due to tool revision, UMC will no longer maintain this flow.

Customer may still download the datasheet and workbook from UMC website for references, but UMC will not provide the databases or scripts mentioned in above documents.

For tool usage issues in the flow, customer may contact local application engineers of related EDA vendors.

Thanks for your kind understanding.

UMC Reference Flow Development Team

**DATASHEET****UMC-Synopsys Digital Reference Flow**

The UMC-Synopsys digital reference flow is a hierarchical design flow used to address multimillion gate designs with high timing complexity. This flow allows designers to shorten their design time by eliminating painful iterations, and lets designers work in parallel by dividing up a large-sized IC. Based on a unified Milkyway database and consistent timing engine, designers can have confidence in achieving good quality results. A reference design is also available to exercise this digital reference flow.

This reference flow demonstrates a complete solution from RTL to verified GDSII using Synopsys tools. It also provides concepts of the design flow steps such that it can be implemented or adapted to any customer design environment. This reference flow is divided into three phases: Design Planning, Design Implementation and Design Refinement & Chip Finishing.

**Phase 1: Design Planning**

A design is converted from RTL to gate netlist. Floorplanning is performed to obtain a realistic chip level planning. Soft macros and their timing budgets are created in the floorplanning step.

**Phase 2: Design Implementation**

A detailed implementation of the chip that achieves timing closure for blocks is performed at this stage. Physical optimization, scan ordering & stitching, clock tree synthesis, detail routing, RC extraction, STA and post route optimization are performed for both block and top levels.

**Phase 3: Design Refinement and Chip Finishing**

Full chip implementation is refined to achieve the final timing closure and to ready chip tapeout. Block and top-level IPO & ECO routing are performed. Final chip-level static timing analysis and physical verification assure a working and clean GDSII for tapeout.

# UMC-Synopsys Digital Reference Flow Chart

