UMC-CADENCE Analog Reference Flow

The UMC-Cadence Analog Reference Flow streamlines the process of designing analog/MM chips targeted to UMC processes. The flow has been proven through silicon and package validation of a test design in a 0.18um MM process. By taking advantage of UMC process technology and Cadence Virtuoso® Custom Design Platform, designers can benefit from a fast, accurate design flow that reduces time-to-silicon and avoids costly re-spins.

KEY BENEFITS
- Improves productivity by providing a reference design environment, baseline flow, and an example design (4-bit DAC) that demonstrates to designers how to use UMC process technology and the Cadence Virtuoso Platform
- Ensures that designs are compatible with Cadence Virtuoso Platform and UMC process technologies, resulting in reliable silicon and an optimized design
- Delivers a predictable path to silicon that can result in shorter design cycles, eliminate costly re-spins
- Provides a tested starting point for building customized design flows
- Reduces development risk, minimizes start-up time, and provides quicker time-to-market

UMC-CADENCE Reference Flow
The UMC-Cadence Analog Reference Flow provides analog and custom designers with an optimized and predictable schematic-to-GDSII flow that has been proven all the way from design, layout, silicon, and measurements. This test design is based on a 4-bit current-steering DAC that utilizes the UMC 0.18um MM PDK, and provides a starting point for design teams who are creating SoCs or putting together a flow of their own.

The collaboration between UMC and Cadence in the development of the reference flow was initiated to improve design efficiency, yield and Turn-around-Time. Companies that are interested in integrating part or all of the reference methodology into their design environment can do it themselves or get assistance from Cadence Engineering Services on an as-needed basis.
Figure 1. Overview of the UMC-Cadence Analog Reference Flow.
The following design tools from the Virtuoso Platform were used to design and verify the 4-bit DAC example highlighted in this document. They represent a subset of the overall Cadence Virtuoso platform, and are appropriate for providing an assessment of designs created using the UMC 0.18um MM PDK. By using composite offering of components from the Cadence Virtuoso platform, the UMC PDK can be examined from schematic capture to layout, and through verification and parasitic re-simulation.

**UMC PDK**

UMC PDK is a foundry design kit created to build a bridge between design and foundry, and shorten analog, mixed-signal design cycles. The process design kit includes schematic symbols, techfiles, callback function for design parameters, parameterized cells for custom layout, schematic-driven layout automation, and provides an easy link to the DRC/LVS/LPE rule deck.

**Virtuoso® Schematic Editor**

Virtuoso Schematic Editor is a full-featured, well-proven schematic capture environment capable of supporting digital, analog, and RF integrated circuit designs within the same environment. Through DFI-based connected libraries, schematics are seamlessly linked to simulation, layout, verification, and parasitic re-simulation in a continuous, seamless flow.

**Virtuoso® Analog Design Environment**

Virtuoso Analog Design Environment is an industry standard platform that supports a variety of analog simulators, and provides the flexibility to use different simulators on the same design. ADE supplies many unique features and is well-suited for use with Virtuoso Spectre Circuit Simulator, and also supports a range of third-party simulators. ADE features an easy-to-use environment for controlling simulation, as opposed to putting simulation control directly on the schematic.

**Virtuoso® Spectre Circuit Simulator**

Spectre is a robust, Spice-like circuit simulator that is well-suited for handling larger circuits and performing convergence on the most difficult ones. Spectre provides tighter integration into Virtuoso Analog Design Environment than any other simulator. Virtuoso Spectre Circuit Simulator supports Verilog-A analog behavioral modeling, which is useful for shortening simulation times and facilitating top-down design. In addition, Virtuoso Spectre Circuit Simulator supports a FastMOS feature that uses table models to speed up simulation times while retaining reasonable accuracy levels.

**Virtuoso®-XL Layout Editor**

Virtuoso- XL Layout Editor is a full-featured physical block layout editor. Virtuoso XL Layout Editor improves productivity by providing a connectivity and design-rule-driven (DRD) layout editing environment. Virtuoso XL Layout Editor takes advantage of the pCells developed within the UMC design kit to rapidly complete circuit block layouts.

**Assura™ DRC and LVS**

Assura DRC and LVS are connected verification tools that are targeted to sub-micron designs. The hierarchy tools are capable of handling multiple levels of layout hierarchy in a fast and reliable manner. Assura DRC and LVS are capable of handling multiple netlist formats, and provide a fast and efficient full-chip locator. Error reporting is performed in a hierarchical manner, allowing faster identification of problem areas.

**Assura™ RCX**

Assura RCX is a 3-D mixed-signal parasitic extraction tool capable of extracting RCLK parasitics from the process physical properties of the layout. AssuraRCX is capable of working with a variety of processes, and is known for combining accuracy with speed.
Figure 2. Screen capture of 4-bit DAC Virtuoso analysis.

AVAILABILITY AND SUPPORT

Registered users can access the
UMC-Cadence Analog Reference Flow kit, Physical Verification &
Extraction Rule Decks, and
simulation models from MyUMC
(www.umc.com)

For further information on the
UMC-Cadence Analog Reference Flow, please contact
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