**Design Support Solutions**

**Overview**

UMC’s Design Support Solutions provide customers with a practical and cost effective environment from RTL designs to GDS2 tape-outs. The fundamental IP solutions include speed and area optimized standard cell libraries, I/O libraries with patented ESD protection, and embedded memory compilers. The platform-based IP solutions enable customers to easily develop specific products such as baseband chips, DTV controllers, audio player controllers, digital camera controllers, etc. The low power design flow provides customers with a quick start for SoC designs in advanced technologies. Cost effective DFM solutions offer customers practical DFM methodologies that are seamlessly compliant with current SoC designs flows. The foundry design kits provide customers a quick and convenient analog design environment with Optimized Capacitor Finder (OCF), Optimized Inductor Finder (OIF) and Optimized Transformer Finder (OTF).

**Fundamental IP**

**Standard Cell Libraries**

UMC’s standard cell libraries are optimized for UMC’s advanced technologies including 90nm, 65nm, 40nm 28nm 22nm and 14nm. They provide rich features including multiple threshold voltage support, over-drive capabilities, density up to 6000 K-gate/mm² at 14nm, multi-Vdd operations, and DFM compliance.

**Standard I/O Libraries**

With patented ESD protection techniques, UMC’s standard I/O libraries provide the best functionality for SoC connectivity. In addition to 16mA fan-out driving, the I/O cells have a compact cell area at advanced nodes with Bonding Over Active Circuit (BOAC) support. Analog I/O & power cells are also available.

**Embedded Memory Compilers**

Embedded memories are generally required for SoC designs. UMC offers complete embedded memory generators for designers’ convenience. These include single port SRAM, dual port SRAM, 1-port register files, 2-port register files, and ROM. The bit cells are built with HVt or RVt MOS transistors for low power designs in advanced technologies.
**ANALOG IP**

**PLATFORM BASED IP SOLUTIONS**
With a complete platform based IP portfolio, customers are able to seamlessly deploy their required IP for specific SoC products, such as baseband SoCs, digital TV controllers, camera controllers and audio players.

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**EMBEDDED MEMORY MACROS**

In the modern SoC era, memory becomes an important and essential IP requirement for SoC design. UMC offers state-of-the-art embedded memory solutions to meet a variety of applications for 4C markets.

High quality embedded non-volatile memory (eFuse, eOTP, eMTP, eEEPROM and eFlash) can be used for trimming, redundancy, data encryption, ID, coding and programming.

In addition, UMC’s proprietary URAM™ is an ideal solution for higher density memory requirements. The important features of URAM are smaller form factor, higher bandwidth/speed and lower power consumption compared to traditional embedded 6T-SRAM.

**UMC EMBEDDED MEMORY PROFILES**

UMC offers a comprehensive embedded memory profile. Customers have many options to help customize their SoC designs.

Furthermore, UMC embedded memory is logic process compatible. The logic standard cell (SC) and I/O can be adopted directly into UMC embedded memory.
**Low Power Design**

With today’s proliferation of low power applications, lowering energy consumption without sacrificing performance has become a critical concern for chip designers. For advanced low power solutions, UMC provides low power kits as well as UMC libraries. Related reference EDA flows are also available upon request. These resources provide customers with a streamlined path to manufacturing, allowing UMC customers designing power-efficient SoC projects to capitalize on today’s low power market opportunities.

### Low Power Design Support

To reduce overall power consumption, designers have to take action during both front-end and back-end design stages. As shown in the following chart, UMC is delivering convenient design solutions to support designers at each stage.

![Power Consumption Trends](chart)

**Power Consumption Trends**

- **Leakage Power**
- **Dynamic Power**

- **Technology Nodes**
  - 0.25um
  - 0.18um
  - 0.13um
  - 90nm
  - 65nm
  - 40nm
  - 28nm
  - 22nm

#### Front-end Design

- **Low leakage process**
  - 80%

- **Power gating**
  - 60%

- **Multi Vth**
  - 40%

- **Multi VDD**

- **Voltage and frequency scaling**

#### Back-end Design

- **Multi Vth**
  - 20%

- **Low power synthesis**

- **Clock gating**
  - 20%

- **Body bias**
  - 40%

- **Voltage and frequency scaling**
  - 60%

- **Multi VDD**

#### Power Saving

- **Leakage Power Saving**

- **Dynamic Power Saving**
  - 80%
## Low Power Design Solutions

<table>
<thead>
<tr>
<th>Type</th>
<th>Support Features</th>
<th>Support</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>14nm 22nm 28nm 40nm 65nm 90nm 0.13um</td>
</tr>
<tr>
<td>Dynamic Power</td>
<td>Voltage Island &amp; Scaling</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Level Shifters w/ Insulator</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Power &amp; Timing Model @ 80% of Vdd</td>
<td>✓</td>
</tr>
<tr>
<td>Clock Gating &amp; Frequency Scaling</td>
<td>Clock Gated F/F</td>
<td>✓</td>
</tr>
<tr>
<td>Leakage Power</td>
<td>Multi-Vt</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Multi-Vt cells</td>
<td>✓</td>
</tr>
<tr>
<td>Power Gating</td>
<td>Isolation cells, Retention F/F Headers / Footers, etc.</td>
<td>✓</td>
</tr>
<tr>
<td>Body Bias</td>
<td>Tapless cells</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Timing / Power Model (i)</td>
<td>✓</td>
</tr>
</tbody>
</table>

Timing and power models will be supported according to each customer’s particular requirements.

## Digital Reference Design Flows

Digital Reference Design Flows provide EDA design methodologies to help customers’ time-to-market. They incorporate EDA vendors’ standard flows to support the digital design implementation process, from RTL to GDSII. The Digital Reference Design Flow design data and document are available in ITC. Your Account Manager can apply the TIC document number for you if you are interested in the details.

## Analog Mixed Signal Reference Flows

UMC’s Analog Mixed Signal Reference Flows provide EDA design methodologies to help accelerate customers’ time-to-market. They incorporate EDA custom design tools to support the full Analog Mixed Signal design process, from schematic to GDS. Analog Mixed Signal Reference Flow design data and documents are available in the TIC system. Your account manager can apply for the TIC document number if you are interested in the details.
**Foundry Design Kit (FDK)**

The Foundry Design Kit provides IC designers with an automatic design environment that eliminates unnecessary manual tasks and ensures successful mixed signal and RF IC tape-outs. The FDK includes parameterized cells (P Cell), which have a schematic layout to provide an automatic and complete design flow. Callback functions are also provided in the design flow to minimize data entry.

In addition, UMC has worked with industry leading EDA tool partners to deliver fast and accurate 3D electromagnetic simulation tools for RF chip designs, including Virtual Capacitor Library (VCL), Virtual Inductor Library (VIL), and Virtual Transformer Library (VTL). UMC has also implemented Optimized Capacitor Finder (OCF), Optimized Inductor Finder (OIF), and Optimized Transformer Finder (OTF) tools deployed inside UMC’s Foundry Design Kit (FDK). These tools allow customers to make tradeoff decision between impedance and area, Q and area, or request a specified “flatness” of inductance within a given frequency range for ultra-wideband (UWB), WiMAX, and mobile TV design.

**Using OIF for Optimum Inductor**
## Broad EDA Tool Support

UMC works closely with leading EDA tool vendors to provide a convenient, productive and up-to-date work environment for designers. Tools are well supported by UMC and its EDA partners throughout the entire design process, from RTL design to tapeout.

<table>
<thead>
<tr>
<th>Logic Design</th>
<th>Physical Design</th>
<th>Physical Verification</th>
<th>ESD/LU Verification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Logic Simulation</strong></td>
<td><strong>PLACE &amp; ROUTE</strong></td>
<td><strong>Verification</strong></td>
<td><strong>DRC</strong></td>
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<tr>
<td>Cadence</td>
<td>Cadence</td>
<td>INNOVUS</td>
<td>Cadence</td>
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<td>Mentor</td>
<td>ModelSim</td>
<td>TEMPUS</td>
<td>Cadence</td>
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<tr>
<td>Synopsys</td>
<td>VCS</td>
<td>VOLTUS</td>
<td>Voltus/Votus-Fi</td>
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<tr>
<td>Synopsys</td>
<td>Synopsys</td>
<td>IC compiler/IC Compiler II</td>
<td>MENTOR</td>
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<tr>
<td></td>
<td></td>
<td>PrimeTime</td>
<td>Synopsys</td>
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<td><strong>Logic Synthesis</strong></td>
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<tr>
<td>Cadence</td>
<td>GENUS</td>
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<tr>
<td>Synopsys</td>
<td>Design Compiler</td>
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</tr>
</tbody>
</table>

### EDA Vendors

- **Cadence**
  - Virtuoso Schematic Editor
  - Spectre
  - SpecterRF
  - Virtuoso
  - Virtuoso XL
  - PVS
  - QRC
  - Voltus/Votus-Fi
  - Redhawk/Totem

- **Mentor Graphics**
  - Eldo
  - Eldo RF
  - Calibre
  - XRC/xACT

- **Keysight Technologies**
  - ADS
  - ADS

- **Synopsys**
  - Custom Compiler
  - HSPICE
  - Laker
  - Custom Compiler
  - ICV
  - StarRC-XT
  - Redhawk/Totem

### Customer Support

- **Partnership with broad IP ecosystem**
  - Enables prompt response from IP vendors
  - Feasibility assessment for customer’s requirements

- **Free Libraries for cost-sensitive products**
  - Foundry library programs

- **UMC Online support environment**
  - IP Master sourcing
  - IP Help Desk
New Customers
For new customer inquiries, please direct all questions to sales@umc.com

Worldwide Contacts
Headquarters:
UMC
No. 3, Li-Hsin 2nd Road, Hsinchu Science Park, Hsinchu, Taiwan, R.O.C.
Tel: 886-3-578-2258
Fax: 886-3-577-9392
Email: foundry@umc.com

In China:
HeJian Technology (Suzhou)
No. 333, Xinghua Street, Suzhou Industrial Park, Suzhou, Jiangsu Province 215025, China
Tel: 86-512-65931299
Fax: 86-512-62530172

United Semiconductor (Xiamen)
No. 899, Wan Jia Chun Road, Xiang An, Xiamen, Fujian 361101, China
Tel: 86-592-7687888

In Japan:
UMC Group Japan
15F Akihabara Centerplace Bldg., 1 Kanda Aoi-Choi Chiyoda-Ku
Tokyo 101-0029 Japan
Tel: 81-3-5294-2701
Fax: 81-3-5294-2707

In Singapore:
UMC-SG
No. 3, Pasir Ris Drive 12, Singapore 519528
Tel: 65-6213-0018
Fax: 65-6213-0005

In Korea:
UMC Korea
1117, Hanshin Intervally24, 322, Teheran-ro, Gangnam-gu, Seoul, Korea
Tel: 82-2-2183-1790
Fax: 82-2-2183-1794
Email:korea@umc.com

In North America:
UMC USA
488 De Guigne Drive, Sunnyvale, CA 94085, USA
Tel: 1-408-523-7800
Fax: 1-408-733-8090

In Europe:
UMC Europe BV
De entree 77
1101 BH Amsterdam Zuidoost
The Netherlands
Tel: 31-(0)20-5640950
Fax: 31-(0)20-6977826

For more information: visit www.umc.com or e-mail sales@umc.com