Mixed-Signal/RFCMOS
Mixed-Signal and RFCMOS applications have become major requirements for system-on-chip designs. UMC provides a logic compatible process for Mixed-Signal/RF solutions and offers many advanced features to optimize the passive devices such as inductors and capacitors. The frequency range of UMC’s scalable models range up to 20GHz. In addition, UMC works very closely with industry leading EDA vendors to deliver seamless design flows to help accelerate time-to-silicon.

**Solutions for Mixed-Signal/RFCMOS Applications**

UMC offers solutions for Mixed-Signal/RFCMOS applications with various data rates. The RF/Wireless Landscape diagram illustrates the data rates and corresponding technologies such as 802.11ay, 802.11ad, 802.11ac, 802.11n, 802.11a/g, 802.11b, 802.11ah, 802.11n, and 802.11ac, among others. The technologies are categorized by Range (from <1m to 50km) and Data rate (10 Gbps, 1 Gbps, 100 Mbps, 10 Mbps, and 1 Mbps). PAN, LAN, and WAN are also indicated with their respective data rates and ranges.
## Technology and Performance

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<thead>
<tr>
<th>Technology</th>
<th>250nm</th>
<th>180nm</th>
<th>130/110nm</th>
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<tr>
<td>IoT/Smart IoT/AIoT</td>
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<td>▲</td>
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</table>

▲ Developing

## Key Features
- High Q inductors on the thicker top copper metal
- High density MIM capacitors
- Cost effective Metal Oxide Metal capacitors (MOM)
- Precision poly resistors
- Deep Nwell for noise isolation
- Multiple Vt devices for optimized circuit performance
- Wide tuning range Varactors
- Diodes
Comprehensive MS/RF Platform

UMC’s MS/RF technology solutions offer optimum speed and performance. UMC’s superior fT and low NFmin satisfy most commercial applications. For portable and consumer applications, UMC provides comprehensive processes in accordance with customers’ particular product requirements.

UMC RFCMOS Process Platform

<table>
<thead>
<tr>
<th>RFCMOS Technology</th>
<th>Process Baselines</th>
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<td></td>
<td>FFC</td>
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<tr>
<td>14nm</td>
<td>Δ</td>
</tr>
<tr>
<td>22nm</td>
<td>-</td>
</tr>
<tr>
<td>28nm</td>
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<td>40nm</td>
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<td>55nm</td>
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<tr>
<td>90nm</td>
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<td>0.11um*</td>
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<td>0.13um</td>
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<tr>
<td>0.18um</td>
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<tr>
<td>0.25um</td>
<td>-</td>
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</table>

- FFC: FinFet Compact
- HPC+: High Performance Compact Ultra
- HPC+: High Performance Compact Ultra Plus
- HLP: High Performance Low Power
- LP: Low Power
- G: Generic
- LL: Low Leakage
- SP: Standard Performance
- HS: High Speed
- GII: General Enhance
- ULP: Ultra Low Power
- GLL: Ultra Low Leakage
- ▲: Developing
- ▲: Available
- *: UMC’s 0.11um AE process with Aluminum BEOL

UMC MS/RFCMOS Offerings

- MOS
  - Native MOS
  - Bipolar
- Active

- MOM
  - Inductor
  - Resistor
  - Diode
- Passive

- MIM
  - Transformer
  - Varactor
  - Transmission Line

- RF Model
  - Monte Carol Model
  - Flicker Noise Model
  - Mismatch Model
  - High Frequency Noise Model
- SPICE Models

- Device Symbols
  - Models
  - P Cells
  - VIL/VCL/VTL
  - Rule decks / Tech Files
- FDK

Note: VIL/VCL/VTL is Virtual Inductor/Capacitor/Transformer Library
FDK is Foundry Design Kit
## 28HPC^+ MS/RF Technology Platform

### Core Devices
- uLVT 0.9V
- LVT 0.9V
- SVT 0.9V
- HVT 0.9V
- uHVT 0.9V
- eHVT 0.9V

### I/O Devices
- 1.8V I/O*
- 2.5V I/O*

### Mixed Signal
- NVT
- Bipolar
- LDMOS
- Diode
- MIS Varactor
- Resistor
- MOM

### RF
- Inductor
- Transformer
- Transformer Line

- **RF Mode (<30GHz) Support**
- **Mixed Signal Support**
- **mm-Wave Support**

* 18V IO: UD 1.5V/1.2V option
** 2.5V IO: OD 3.3V, UD 2.5V/1.8V option

---

## Active and Passive Devices

<table>
<thead>
<tr>
<th>Active Devices</th>
<th>L130E</th>
<th>L101AE</th>
<th>90LL</th>
<th>90SP</th>
<th>L65LL</th>
<th>L65LP/SP</th>
<th>L55LP/ULP</th>
<th>40LP/ULP</th>
<th>28HLP</th>
<th>28HPC*</th>
<th>28HPC^+</th>
<th>22ULP</th>
<th>22ULL</th>
<th>14FFC</th>
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<th>Active Devices</th>
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<th>28HLP</th>
<th>28HPC*</th>
<th>28HPC^+</th>
<th>22ULP</th>
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▲ Available
**Foundry’s First Virtual Inductor/Transformer/Capacitor Libraries**

UMC works with its EDA tool partners to deliver the industry's first parameterized design kits. Full wave simulation has been performed on all kits within the Virtual Inductor / Transformer / Capacitor Libraries. The virtual libraries enable RFCMOS designers to create and simulate custom inductor geometries that are based on UMC’s processes. These libraries are built upon UMC’s Electromagnetic Design Methodology (EMDM), which allows engineers to easily and accurately create any RF structure. EMDM gives designers the flexibility to innovate new geometries simply by editing parameters such as diameter, number of turns or width.

**Foundry’s First Virtual Library**

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<thead>
<tr>
<th>VIL</th>
<th>VTL</th>
<th>VCL</th>
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<tbody>
<tr>
<td>Spiral</td>
<td>W/O center tap</td>
<td>Symmetry</td>
</tr>
<tr>
<td>Differential w/o center tap</td>
<td>CT on primary coil</td>
<td>Asymmetry</td>
</tr>
<tr>
<td>Differential with center tap</td>
<td>CT on secondary</td>
<td>Octagon</td>
</tr>
<tr>
<td>Stack</td>
<td>CT on both coils</td>
<td>• Input: single/differential end</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Output: single/differential end</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Turn Ratio: 1:n, n:2n, n:n</td>
</tr>
</tbody>
</table>

*Note: The Virtual library can be used to simulate all types of RF inductors and capacitors. CT: Center Tap*

**MS/RF Design Flow and FDK**

The FDK (Foundry Design Kit) provides IC designers with an automatic design environment. The methodology provides access to circuit-level design and simulation, circuit layout, and layout verification using RF device models. In the front-end, fundamental components of UMC’s MS/RF process are implemented in common design environments and simulation tools. The back-end includes parameterized cells (P Cell), which includes a schematic driven layout to provide an automatic and complete design flow. Callback functions are also provided in the design flow to minimize data entry. EDA tools for MS/RF designs are also supported.
UMC offers the Optimum Inductor Finder (OIF) in the FDK package. The OIF gives designers the ability to quickly access a large library of inductors accurately calibrated to UMC's silicon. It also allows users to perform inductor optimization through just a few simple steps using the user-friendly interface. For instance, customers can define a desired inductor and make trade-offs between Q-factor and area. The OIF will select a design that best fits the specifications in a matter of seconds.

In addition, UMC offers the Optimum Capacitor Finder (OCF) in the FDK package. The OCF gives designers the ability to quickly access a large library of capacitors accurately calibrated to UMC's silicon. It also allows users to perform capacitor optimization through just a few simple steps using the user-friendly interface. For instance, customers can define a desired capacitor and make trade-offs between Q-factor and area. The OCF will select a design that best fits the specifications in a matter of seconds.

UMC also offers the Optimum Transformer Finder (OTF) in the FDK package. The OTF gives designers the ability to quickly access a large library of transformers accurately calibrated to UMC's silicon. It also allows users to perform transformer optimization through just a few simple steps using the user-friendly interface. For instance, customers can define a desired transformer and make trade-offs between impedance and area. The OTF will select a design that best fits the specifications in a matter of seconds.

**FDK EDA Supported Tools**

<table>
<thead>
<tr>
<th>Design Flow</th>
<th>Cadence</th>
<th>Mentor</th>
<th>ADS</th>
<th>Synopsys</th>
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<td>Schematic Entry</td>
<td>Composer</td>
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<td>ADS*</td>
<td>Laker ADP*</td>
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<td>Pre-simulation</td>
<td>SpectreRF</td>
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<td>GoldenGate*</td>
<td>HSPICE</td>
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<tr>
<td>Hspice/Spectre Models</td>
<td>Virtuoso XL</td>
<td></td>
<td>Laker L3*</td>
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<tr>
<td>Physical Design</td>
<td>Assura QRC</td>
<td>Calibre XRC</td>
<td>Hercules Star RCXT</td>
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<tr>
<td>Physical Verification (DRC/LVS/RCX)</td>
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</tbody>
</table>

Note: * is available by request
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For new customer inquiries, please direct all questions to sales@umc.com

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