

Notice in Usage of This Reference Flow

Dear Valued Customer,

Due to tool revision, UMC will no longer maintain this flow.

Customer may still download the datasheet and workbook from UMC website for references, but UMC will not maintain the databases or scripts mentioned in above documents.

For tool usage issues in the flow, customer may contact local application engineers of related EDA vendors.

Thanks for your kind understanding.

UMC Reference Flow Development Team



DataSheet

UMC-Synopsys 90nm Multi-Vt Reference Design Flow

UMC-Synopsys 90nm Multi-Vt reference design flow is a fully validated hierarchical design flow to address multimillion gate designs with high timing complexity. This flow allows designer shorten their design time by eliminating painful iterations, and it lets designers work in parallel by dividing up a big chip. Based on a unified Milkyway™ database and consistent timing engine, designers can have confidence in achieving good quality of results.

The reference design flow demonstrates a complete solution from RTL to verified GDSII using Synopsys tools, UMC 90nm process and LEON2 32-bit RISC core. It provides concepts of the design flow steps such that it can be implemented or adapted to any customer design environment. This reference flow also supports sub flows to allow soft and hard block integrations.

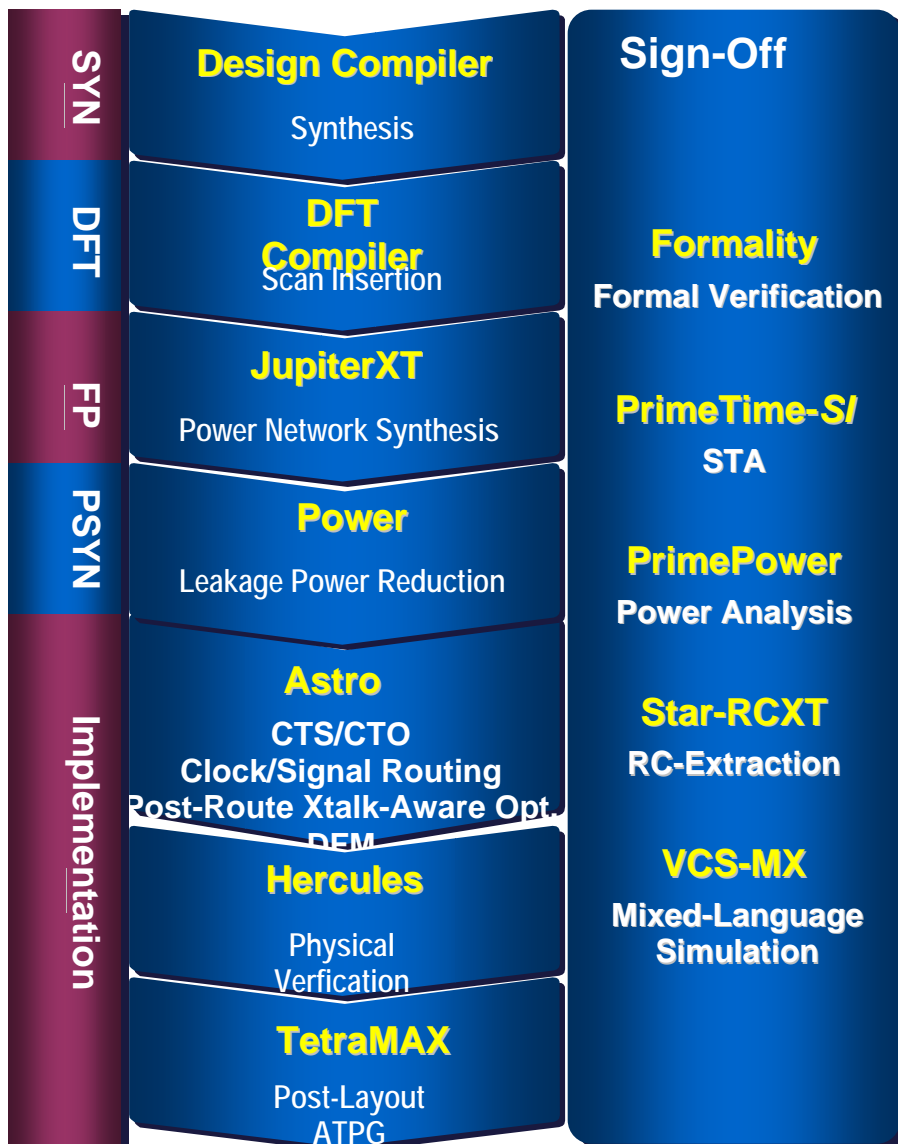
Framework for High-Performance Designs

The reference design flow is based on the Synopsys Galaxy™ Design and Discovery™ Verification Platforms, which include Jupiter-XT™ for design planning, Physical Compiler® for unified synthesis and placement, Astro™ for physical implementation, Primetime® and Primetime-SI® for full-chip timing analysis, and Hercules for physical verification. The flow supports the Liberty™ library open source formats and other standard formats.

Highlights

- Built on Synopsys Galaxy™ Design and Discovery™ Verification Platforms by Synopsys Professional Services based on production proven design methodology
- Utilized the LEON2 32-bit RISC CPU, developed by Gaisler Research, as a reference design. The core consists of a SPARC-V8 compliant 32-bit RISC CPU, industrial standard AMBA system buses, 10/100 Ethernet MAC, and industrial standard PCI interfaces. It is highly configurable and expendable to plug-in additional digital and/or AMS hard IP's.
- Enables designers to resolve VDSM design bottlenecks associated with power network synthesis, power network analysis, IR drop and electro-migration (EM) analysis, signal integrity (SI) and crosstalk analysis

- Supports critical UMC 90nm design for manufacturing (DFM) design rules and design guidelines using Synopsys Astro physical implementation tool
- Supports multiple hierarchical design approach to address chip complexity and enable efficient management and sharing of large amount of design data



UMC-Synopsys 90nm Reference Design Flow Diagram