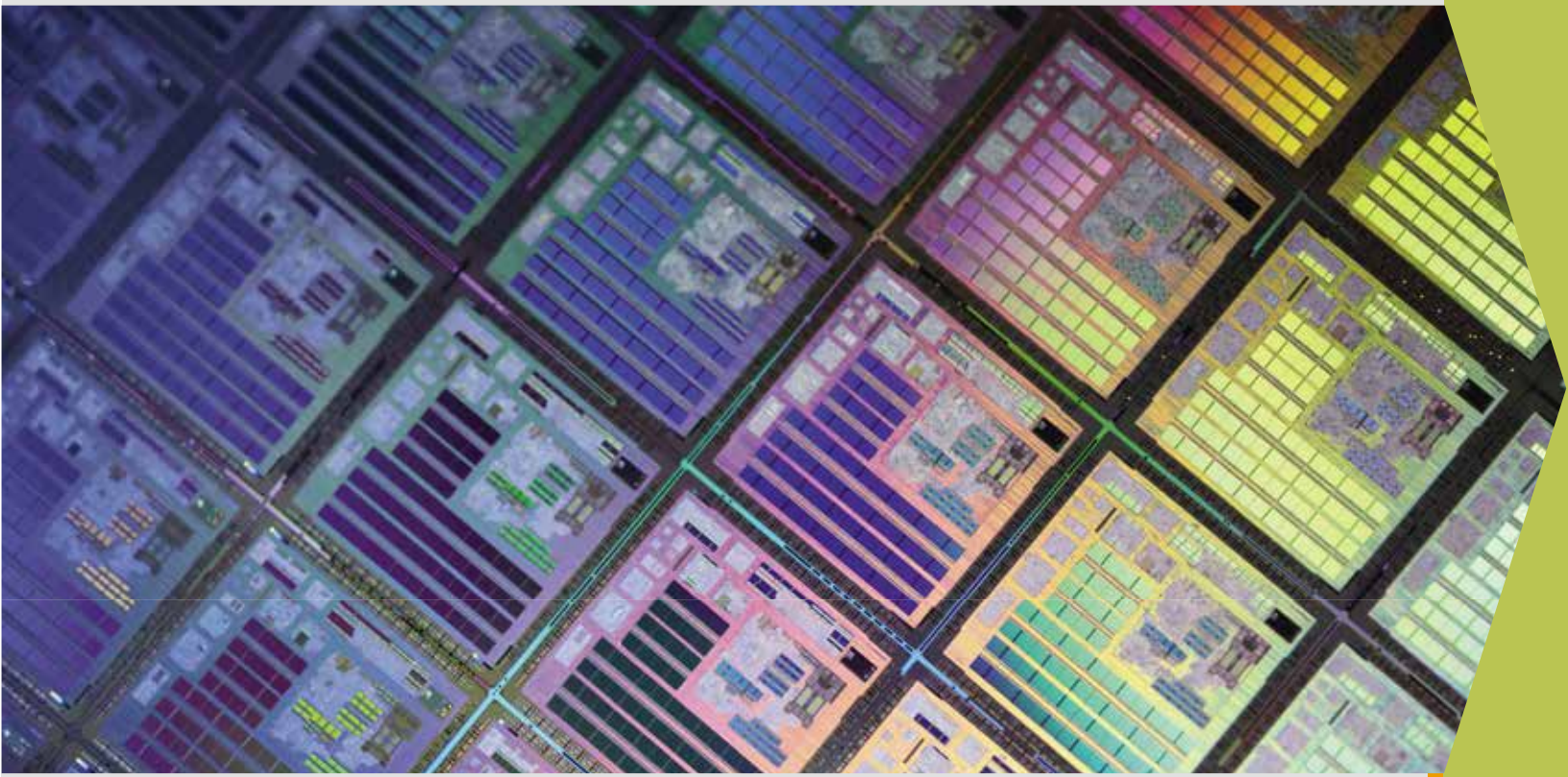


FOUNDRY LEADERSHIP FOR THE SoC GENERATION

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28 NANOMETER

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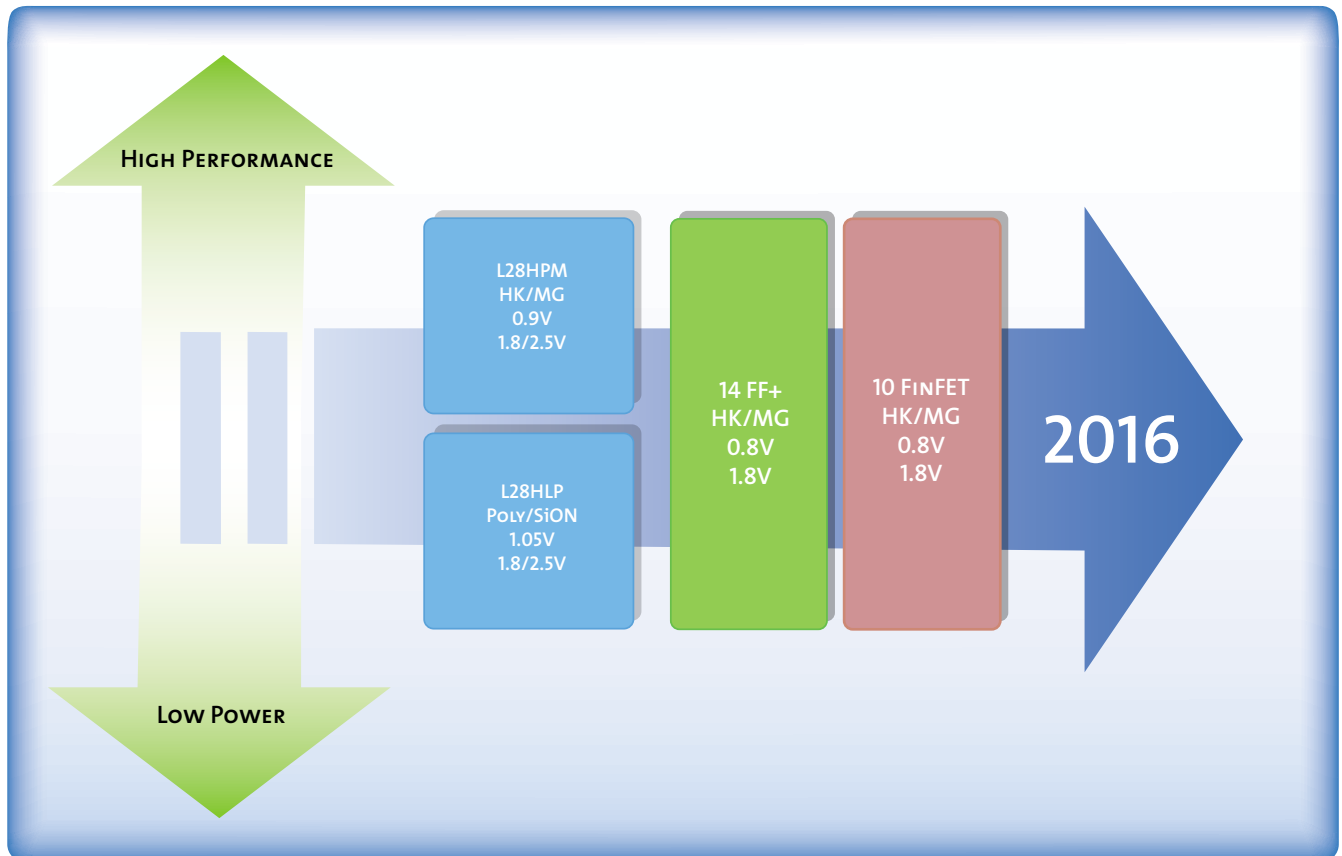


UMC

28 NANOMETER

UMC's 28nm process technology is developed for applications that require the highest performance with the lowest power leakage. In October 2008, we were the first foundry to deliver fully functional 28nm SRAM chips and have proven in silicon the high-K/metal gate technology used for this technology node. Our 28nm platform is based on industry mainstream technology that includes conventional poly/oxynitride process and gate last, high-K metal gate, which provides superior performance over gate first high-k offerings. Currently, our 28nm is in volume production for several customer products.

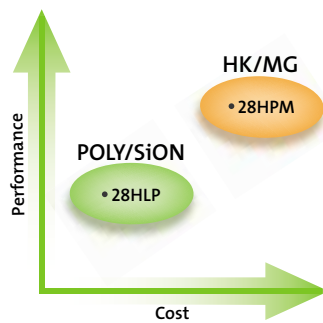
ADVANCED TECHNOLOGY ROADMAP



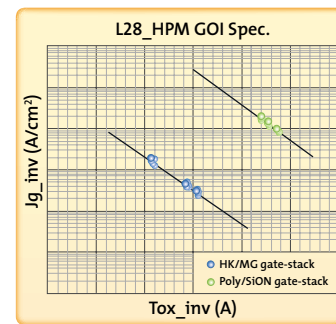
28NM TECHNOLOGY FOR BROAD APPLICATIONS

UMC incorporates multiple approaches for its 28nm technology to address different market applications. The first option is conventional poly-SiON technology used for our High-Performance Low Power (HLP) processes. The HLP process delivers a 10% performance enhancement over the industry standard platform due to process optimization techniques. These platforms are ideal for portable applications and consumer electronics such as mobile phones, wireless ICs and TVs. For applications that require performance enhancement but still maintain low power consumption, a second, High-K/Metal Gate (HK/MG) option is offered on a High Performance for Mobile (HPM) platform. The HPM process is ideal for speed-intensive and power consumption optimization products such as digital TV applications, portable processors and high speed networking.

28NM PLATFORM COST VS. PERFORMANCE



HK/MG TECHNOLOGY BENEFITS



* Based on UMC's internal benchmarking. Actual customer product performance results will vary.

28NM DEVICE SOLUTIONS

UMC's 28-nanometer solution features a flexible technology design platform. Customers can choose the process device options optimized for their specific application, such as HPM, LP and HLP transistors with their multiple Vt options.

L28 DEVICE OFFERING

PLATFORM OFFERING		HLP	HPM
	CORE VCC (V)	1.05	0.9
VT OPTIONS	ULTRA -LOW		✓
	LOW	✓	✓
	REGULAR	✓	✓
	HIGH	✓	✓
	ULTRA - HIGH		✓
1.8V IO	1.8V UD 1.2V		✓
	1.8V UD 1.5V	✓	✓
	1.8V	✓	✓
2.5V IO	2.5V UD 1.8V	✓	✓
	2.5V	✓	✓
	2.5V OD 3.3V	✓	✓
SRAM	SP	✓	✓
	DP	✓	✓

* OPTIONAL IO OFFERING

IP SUPPORT

Fundamental IPs (standard cells, I/Os, and memory compilers listed below) are optimized to UMC technologies, and are planned for development from several leading vendors to be available free-of-charge (please contact a UMC account manager for more information). Customers can also leverage application specific IPs for DTV, graphics, networking, etc. IPs available through UMC are DFM (Design for Manufacturing) compliant for better manufacturability.

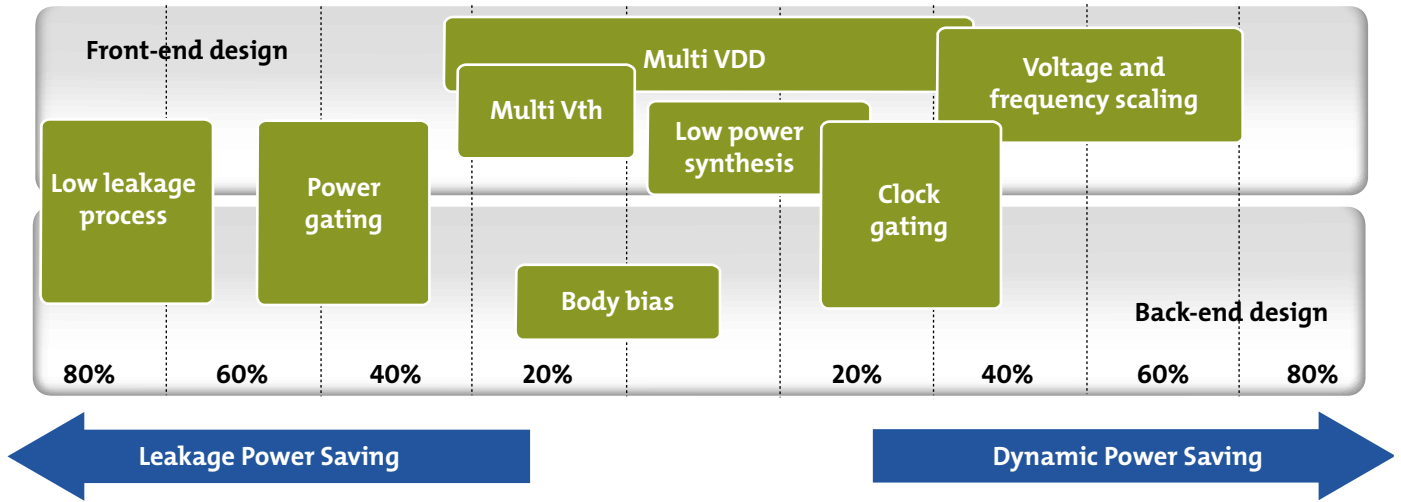
FUNDAMENTAL IP	INTERFACE/FUNCTIONAL IP	
Multi-voltage Standard Cell Library	USB 2.0 pico PHY	USB2.0 480Mbps
1.8V IO Library	USB 3.0 5Gbps	SerDes 12.5Gbps
2.5V IO Library	PCIE Gen II	PCIE GEN III 8Gbps
eFuse 32b~4Kb	SATA3 6G	MIPI D PHY TX & RX
Single Port SRAM Compiler	DDR 3/2 1600MHz	HDMI 1.4a TX & HEAC
Dual Port SRAM Compiler	OTP 8Kb~4Mb	MIPI D-PHY Bi-direction, 2L & 4L
Single Port Register File	MIPI M-PHY Type I, 1T1R	MIPI M-PHY Type I, 2T2R
Dual Port Register File	DDR multi PHY DDR2, 3, 3L, mDDR, LPDDR2 PHY(1066)	
ROM Compiler	PLL with variable input/output frequency ranges	

LOW POWER FEATURES OF STANDARD CELL LIBRARY

With today's proliferation of low power applications, lowering energy consumption without sacrificing performance has become a critical concern for designers of power management chips for portable electronics. UMC supports its standard cell library with low power design features, including multiple Vt, clock-gating, level shifter and other features to complement UMC's complete low power solution.

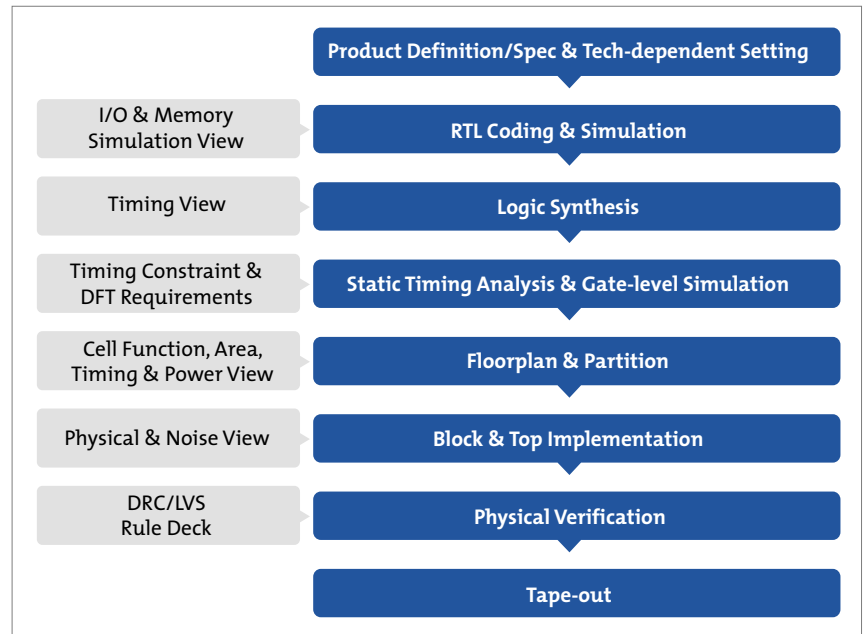
TYPE		SUPPORT FEATURES		SUPPORT				
				28NM	40NM	65NM	90NM	0.13UM
Operating Power	Voltage Island & Scaling	Level Shifters w / Insulator	Power & Timing Model @ 80% of Vdd	√	√	√	√	√
	Clock Gating & Frequency Scaling	Clock Gated F/F		√	√	√	√	√
Leakage Power	Multi-Vt	Multi-Vt cells		√	√	√	√	√
	Power Gating	Isolation cells, Retention F/F Headers / Footers, etc.		√	√	√	√	√
	Body Bias	Tapless cells	Timing / Power Model	√	√	√	√	√

LOW POWER DESIGN SUPPORT



UMC REFERENCE DESIGN FLOW

UMC Reference Design Flow provides a design methodology and flow validated with a “Leon2” system demonstration board. The flow incorporates 3rd-party EDA vendors’ baseline design flows to address issues such as timing closure, signal integrity, leakage power and design for manufacturability and adopts a hierarchical design approach built upon silicon validated process libraries. UMC Reference Design Flow covers from RTL coding all the way to GDS-II generation and supports Cadence, Magma, Mentor and Synopsys EDA tools. All of these tools can be interchanged for added flexibility.



SYNOPTYS®

Mentor
Graphics

cādence®

REFERENCE DESIGN FLOW AND VENDOR SUPPORT

UMC works with leading EDA tool companies to provide a verified Reference Design Flow program to ensure the accuracy of customer designs in a proven environment. UMC's Reference Design Flow program integrates solutions for digital designs and low power solutions that incorporate the latest DFM resources available from leading third-party providers. Tools can be interchanged for added flexibility.

FEATURES OF DESIGN FLOW	CADENCE	SYNOPSIS	MENTOR
Functional Logic Simulation	▲	▲	▲
Schematic Entry	-	-	-
Logic Synthesis	▲	▲	-
Static Timing Analysis	▲	▲	-
Timing Closure	▲	▲	-
Signal Integrity	▲	▲	-
Floor Planning	▲	▲	-
Physical Synthesis	▲	▲	-
Multi-Vt Low Power	▲	▲	-
Multi-Vdd Low Power	▲	▲	-
Design For Test	▲	▲	▲
Design For Diagnosis	▲	▲	▲
DFM - double via insertion	▲	▲	▲
DFM - dummy metal filling	▲	▲	▲
Circuits Simulation	▲	▲	▲
Power Analysis	▲	▲	-
Layout Editor	▲	-	▲
Place & Route	▲	▲	-
Physical Verification	▲	▲	▲
Formal Verification	▲	▲	-
Parasitic Extraction	▲	▲	▲
Noise Analysis	▲	▲	-

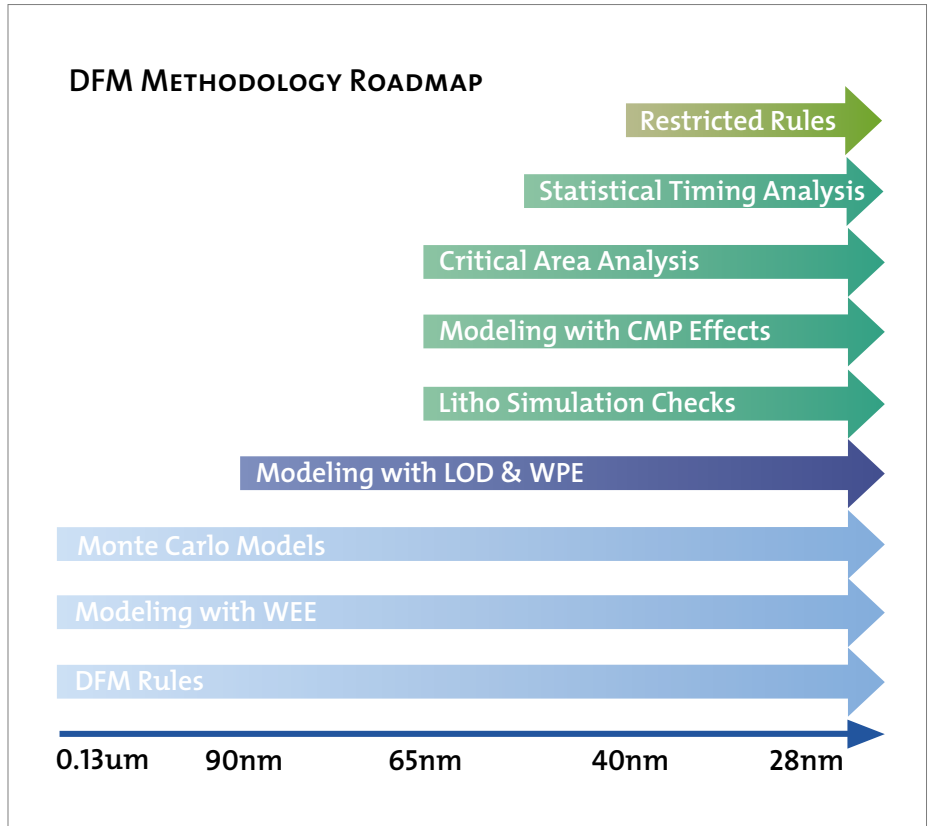
Note: ▲ Available

DFM METHODOLOGY

UMC offers optimal DFM (Design For Manufacturability) solutions to effectively and efficiently address factors that may negatively affect yield and performance for advanced technology designs. UMC's DFM solutions include advanced process models incorporated in SPICE and extraction decks for predicting random and systematic variations, technology files, DFM-compliant libraries and IP that embrace the intricacies of the fabrication process. Concise DFM recommendation rules are available along with a comprehensive rule-deck runset strategy to fulfill various design requirements.

UMC also offers pre-tapeout Optical Proximity Correction (OPC) and Litho Rule Check (LRC) for custom designs in addition to our standard post-tapeout services that include OPC, Litho Simulation Check (LSC), dummy fill, and metal slotting. At 65nm and below, UMC offers a DFM Design

Enablement Kit (DEK) to seamlessly support model-based DFM tools. The DEK has a built-in Graphic User Interface (GUI) for DFM design database setup, and is completed with application notes and qualification reports for design reference.



New Customers

For new customer inquiries,
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